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UTILITY PATENT APPLICATION TRANSMITTAL (Only for new nonprovisional applications under 37 CFR 1.53(b))	Attorney Docket No.	960942A	Total Pages	
	First Named Inventor or Application Identifier			
	Yoshiyuki YONEDA et al.			
	Express Mail Label No.			
Check Box, if applicable [ ] Duplicate	PAGE 1 OF 3			

APPLICATION ELEMENTS FOR:	ADDRESS TO:
DEVICE HAVING RESIN PACKAGE AND METHOD OF PRODUCING SAME	Assistant Commissioner for Patents BOX PATENT APPLICATIONS Washington, D.C. 20231

1. [X] Fee Transmittal Form (Incorporated within this form)
   (Submit an original and a duplicate for fee processing)

2. [X] Specification Total Pages [97]

3. [X] Drawing(s) (35 USC 113) Total Sheets [97]

4. [X] Oath or Declaration Total Pages [3]

   a. [ ] Newly executed (original or copy)

   b. [X] Copy from prior application (37 CFR 1.63(d) (for continuation/divisional with Box 17 completed).

      i. [ ] Deletion of Inventor(s)
      Signed statement attached deleting inventor(s) named in prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. [X] Incorporation by reference (usable if box 4b is checked)
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Microfiche Computer Program (Appendix)

7. [ ] Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)

   a. [ ] Computer Readable Copy
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<u>**ACCOMPANYING APPLICATION PARTS**</u>

8. [ ] Assignment Papers (cover sheet and document(s))

9. [ ] 37 CFR 3.73(b) Statement (when there is an assignee) [ ] Power of Attorney

UTILITY PATENT APPLICATION TRANSMITTAL (Only for new nonprovisional applications under 37 CFR 1.53(b))	Attorney Docket No. 960942A First Named Inventor or Application Identifier Yoshiyuki YONEDA et al. PAGE 2 OF 3

10. [ ] English translation Document (if applicable)
11. [X] Information Disclosure Statement [ ] Copies of IDS Citations
12. [] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503)
14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application Status still proper and desired.
15. [X] Claim for Convention Priority [ ] Certified copy of Priority Document(s)
    a. Priority of Japan application no. 7-290135 filed on November 8, 1995 , of Japan application no. 8-183838 filed on July 12, 1996, of Japan application no. 7-322803 filed on December 12, 1995, of Japan application no. 8-250707 filed on September 20, 1996 and of Japan application no. 8-267607 filed on October 8, 1996 are claimed under 35 USC 119. The certified copies have been filed in prior application Serial No. 08/744,048 (For Continuing Applications, if applicable).
16. [ ] Other ____
17. [X] If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

    [] Continuation [X] Division [ ] Continuation-in-part (CIP) of prior application no. 08/744,048

    a. [X] Please amend the specification by inserting after the title: --This application is a divisional of prior application Serial No. 08/744,048 filed November 6, 1996.--.

    b. [X] Cancel in this application original claims 1, 3, 4, 6, 14, 16, 17, 19, 23-26 and 42-43 of the prior application before calculating the filing fee.

FEE TRANSMITTAL The filing fee is calculated below	Number Filed	Number Extra	Rate	Basic Fee $760.00
Total Claims	36- 20	16	x $18.00	288.00
Independent Claims	5 - 3	2	x $78.00	156.00
Multiple Dependent Claims			$260.00	
			Basic Filing Fee	$1204.00
Reduction by 1/2 for small entity				
Fee for recording enclosed Assignment			$40.00	
TOTAL				$1204.00

UTILITY PATENT APPLICATION TRANSMITTAL (Only for new nonprovisional applications under 37 CFR 1.53(b))	Attorney Docket No.	960942A
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[X] A check in the amount of $ 1204.00 is enclosed to cover the filing fee.

[ ] Please charge our Deposit Account No. **01-2340** in the total amount of $ to cover the filing fee and the $ assignment recordation fee. A duplicate of this sheet is attached.

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18. CORRESPONDENCE ADDRESS

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SUBMITTED BY	
Typed or Printed Name William L. Brooks	Reg. No. 34,129
Signature William L. Brooks	Date: November 17, 1999

SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

BE IT KNOWN THAT WE, Yoshiyuki Yoneda, a citizen of Japan residing at c/o FUJITSU LIMITED, 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa, 211 Japan, Kazuto Tsuji, a citizen of Japan residing at c/o FUJITSU LIMITED, 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa, 211 Japan, Seiichi Orimo, a citizen of Japan residing at c/o FUJITSU LIMITED, 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa, 211 Japan, Hideharu Sakoda, a citizen of Japan residing at c/o FUJITSU LIMITED, 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa, 211 Japan, Ryuji Nomoto, a citizen of Japan residing at c/o FUJITSU LIMITED, 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa, 211 Japan, Masanori Onodera, a citizen of Japan residing at c/o FUJITSU LIMITED, 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa, 211 Japan and Junichi Kasai, a citizen of Japan residing at c/o FUJITSU LIMITED, 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa, 211 Japan have invented certain new and useful improvements in

DEVICE HAVING RESIN PACKAGE AND METHOD OF PRODUCING THE SAME

of which the following is a specification : -

TITLE OF THE INVENTION

DEVICE HAVING RESIN PACKAGE AND METHOD OF PRODUCING THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to devices having a resin package such as semiconductor devices, and more particularly to a resin-sealed semiconductor device of a leadless surface mounting type directed to high-density mounting. Further, the present invention is concerned with a method of producing such a semiconductor device.

Recently, down-sizing of electronic devices has required a decrease in the pitch of leads extending from a resin-sealed type package. Hence, it is desired that there are provided a new structure of the resin-sealed type package making it possible to further decrease the lead pitch and a method of producing such a structure.

2. Description of the Related Art

Figs. 1A, 1B and 1C are diagrams of a semiconductor device having a conventional resin-sealed package. The device includes a resin 1, a chip 2, outer leads 3, bonding wires 4 made of an alloy of gold and aluminum (Au-Al), and a die pad 5. The package shown in Figs. 1A, 1B and 1C is called an SSOP (Shrink Small Outline Package). The outer leads 3 are bent in a gull-wing shape, and are mounted on a circuit board.

Fig. 2 is a cross-sectional view of a semiconductor device of another type. The device shown in Fig. 2 includes solder balls 6 and a mount base 7 on which the chip 2 sealed by the resin 1 and solder balls 6 are provided. The package shown in Fig. 2 is called a BGA (Ball Grid Array) type, and the solder balls 6 serve as terminals provided on the

mount base 7.

The SSOP type package shown in Figs. 1A, 1B and 1C has a disadvantage in which a large area 9 is needed to arrange inner leads 8 integrally formed with the outer leads 3, and a large area is needed to arrange the outer leads 3. Hence, the SSOP type package needs a large mounting area.

The BGA type package shown in Fig. 2 is expensive because it needs the mount base 7.

SUMMARY OF THE INVENTION

It is a general object of the present invention to provide a resin-packaged device and a production method of producing the same in which the above disadvantages are eliminated.

A more specific object of the present invention is to provide a less-expensive resin-packaged device which requires a smaller mounting area and provide a method of producing the same.

The above objects of the present invention are achieved by a device comprising: a chip (111); a resin package (112, 151, 314) sealing the chip, the resin package having resin projections (117, 154, 318) located on a mount-side surface of the resin package; metallic films (113, 155, 315) respectively provided to the resin projections; and connecting parts (118, 101, 163, 245, 313, 341, 342) electrically connecting electrode pads of the chip and the metallic films.

The device may be configured so that each of the metallic films is a single layer (113A) made of a metallic substance.

The device may be configured so that each of the metallic films comprises a plurality of metallic layers (113B - 113D, 213E - 213G) which are stacked.

The device may be configured so that the connecting parts respectively comprise bonding wires (118), which are bonded to the electrode pads and the

metallic films.

The device may be configured so that: the connecting parts respectively comprise bonding wires (118), and bonding balls (101, 245) respectively provided to the metallic films; and the bonding wires are bonded to the electrode pads and the bonding balls.

The device may be configured so that the resin package is a molded package so that the resin projections are integrally formed.

The device may be configured so that the resin package includes a first resin portion (153) on which the chip is provided, and a second resin portion (152) which covers the chip.

The device may be configured so that: the connecting parts respectively comprise bonding wires (118), and connection electrodes (156) which are provided on the first resin portions and extend, into the resin projections, to the metallic films; and the bonding wires are bonded to the electrode pads and the connection electrodes.

The device may be configured so that the resin projections (154) respectively have through holes (157) through which the connection electrodes extend to the metallic films.

The device may be configured so that: the metallic films (315) respectively have lead portions (3151), which are sealed by the resin package and extend toward the chip; and the connecting parts include bonding wires which are bonded to the lead portions.

The device may be configured further comprising a heat radiating member (340) sealed by the resin package, the chip being provided on the heat radiating member.

The device may be configured so that: the connecting members respectively comprise bumps (342)

provided between the electrode pads (312) of the chip (311) and the metallic films (315).

The device may be configured so that: the metallic films (315) respectively have lead portions (3151), which are sealed by the resin package and extend toward the chip; and the connecting parts include bumps (342) provided between the electrode pads (312) of the chip (311) and the lead portions (3151) of the metallic films.

The device may be configured so that: the metallic films (315) respectively have lead portions (3151), which are sealed by the resin package and extend toward the chip, the lead portions (3151) having recess portions (343); and the connecting parts include bumps (342), which are positioned in the recess portions (343) and are provided between the electrode pads (312) of the chip (311) and the lead portions (3151) of the metallic films.

The device may be configured so that a back surface of the chip (311) opposite to a surface on which the electrode pads are provided is exposed from a surface of the resin package opposite to the mount-side surface thereof.

The device may be configured so that it further comprises a heat radiating member (345) attached to the back surface of the chip.

The device may be configured so that it further comprises an insulating member provided to a surface of the chip on which the electrode pads are provided.

The device may be configured so that the connecting parts comprise an electrically conductive resin containing conductive particles (348) joined together under a given pressure.

The above objects of the present invention are also achieved by a device comprising: a chip (111); a resin package (151) sealing the chip and

having a first resin portion (153) and a second resin portion (152), the chip being provided on the first resin portion (153) and covered by the second resin portion; connecting parts (118, 172) having bonding wires (118) and connection electrodes (172), the connection electrodes being provided on the first resin portion (153) and projecting therefrom; and metallic films (155) respectively provided to the connection electrodes of the connecting parts.

The above objects of the present invention are also achieved by a device comprising: a chip (111); a resin package (181) sealing the chip and having a first resin portion (183) and a second resin portion (182), the chip being provided on the first resin portion (183) and covered by the second resin portion, the first resin portions having through holes (184); electrode parts (185) provided to the first resin portion (182) so as to respectively cover the through holes; and connecting parts (118) connecting electrode pads of the chip and the electrode parts (185).

The device may be configured so that the first resin portion comprises a resin tape (183).

The device may be configured so that the connecting parts respectively comprise bonding wires, which are bonded to the electrode pads and the electrode parts (185).

The above objects of the present invention are also achieved by a device comprising: a chip (211); a resin package (212) sealing the chip, the resin package having resin projections (217, 217B) located on a mount-side surface of the resin package, the resin projections extending downwards from the mount-side surface and laterally extending from at least one side surface of the resin package; metallic films (213) respectively provided to the resin projections; and connecting parts (218) electrically

connecting electrode pads of the chip and the metallic films.

The device may be configured so that each of the metallic films is a single layer (113A) made of a metallic substance.

The device may be configured so that each of the metallic films comprises a plurality of metallic layers (113B - 113D, 213E - 213G) which are stacked.

The device may be configured so that the connecting parts respectively comprise bonding wires (218), which are bonded to the electrode pads and the metallic films.

The device may be configured so that: the connecting parts respectively comprise bonding wires (218), and bonding balls (101, 245) respectively provided to the metallic films; and the bonding wires are bonded to the electrode pads and the bonding balls.

The device may be configured so that the resin package is a molded package so that the resin projections are integrally formed.

The device may be configured so that the resin projections (217) laterally extend from a plurality of side surfaces of the resin package.

The device may be configured so that the resin projections (217B) laterally extend from only one side surface of the resin package.

The device may be configured so that it further comprises supporting members (253) provided to the resin package (212), the supporting members (253) supporting the device vertically mounted on a circuit board.

The above objects of the present invention are also achieved by a device comprising: a chip (211); a resin package (212) sealing the chip, the resin package having resin projections (291A, 291B) located on a mount-side surface of the resin package,

the resin projections extending downwards from the mount-side surface and being substantially flush with a side surface of the resin package; metallic films (290A, 290B) respectively provided to the resin projections; and connecting parts (218) electrically connecting electrode pads of the chip and the metallic films.

The device may be configured so that: the resin projections comprise first projections (291A) and second projections (291B) being laterally longer than the first projections so that the second projections extend below the chip; and the metallic films comprise first metallic films (290A) provided on the first projections, and second metallic films (290B) provided on the second projections.

The device may be configured so that it further comprises a spacer (293) to be provided to the mount-side surface of the resin package, so that the spacer is in contact with another device when the device is supported on a circuit board so that the side surface of the resin package faces the circuit board.

The device may be configured so that the spacer is a heat radiating member.

The above objects of the present invention are also achieved by a method of producing devices respectively having chips sealed by resin packages, the method comprising: (a) forming a lead frame (120) having a base (121) having recess portions (122) respectively having metallic films (113); (b) mounting chips (111) on the lead frame; (c) providing connecting parts (118, 101, 163, 245) which electrically connect electrode pads of the chips and the metallic films; (d) molding resin so that molded resin packages respectively cover the chips and metallic films supported by the lead frame; and (e) separating the molded resin packages from the lead

frame together with the metallic films provided to resin projections which are counterparts of the recess portions.

The method may be configured so that the step (e) comprises a step of etching the lead frame and thereby dissolving the lead frame.

The method may be configured so that the step (e) comprises a step of mechanically separating the lead frame from the molded resin packages.

The method may be configured so that it further comprises a step of providing a tape member to the molded resin packages before the step (e) is executed.

The method may be configured so that the step (c) comprises a first step of providing bonding balls to the metallic films, and a second step of bonding bonding wires to electrode pads of the chip and the bonding balls, the bonding balls and the bonding wires corresponding to the connecting parts.

The method may be configured so that the step (d) molds the resin so that the molded resin packages are joined together.

The method may be configured so that the step (d) molds the resin so that the molded resin packages are separated from each other.

The above objects of the present invention are achieved by a device comprising: a chip (311); a resin package (314) sealing the chip, the resin package having a mount-side surface of the resin package; metallic films (315) respectively provided in the resin package so that the metallic films are flush with the mount-side surface and are exposed therefrom; and connecting parts (313, 101, 342) electrically connecting electrode pads of the chip and the metallic films.

The device may be configured so that: the connecting parts respectively comprise bonding wires

(313), and bonding balls (101) respectively provided to the metallic films; and the bonding wires are bonded to the electrode pads and the bonding balls.

The device may be configured so that each of the metallic films is a single layer (315A) made of a metallic substance.

The device may be configured so that each of the metallic films comprises a plurality of metallic layers (315B - 315D) which are stacked.

The device may be configured so that the connecting parts respectively comprise bumps (342) provided between the electrode pads (312) of the chip (311) and the metallic films (315).

The above objects of the present invention are achieved by a method of producing devices respectively having chips sealed by resin packages, the method comprising: (a) forming a lead frame (320) having a base (321) on which metallic films (315) are formed; (b) mounting chips (311) on the lead frame; (c) providing connecting parts (313, 101) which electrically connect electrode pads of the chips and the metallic films; (d) molding resin so that molded resin packages respectively cover the chips and metallic films supported by the lead frame; and (e) separating the molded resin packages from the lead frame together with the metallic films so that the chips are exposed from mount-side surfaces of the molded resin packages.

The method may be configured so that the step (e) comprises a step of etching the lead frame and thereby dissolving the lead frame.

The method may be configured so that the step (e) comprises a step of mechanically separating the lead frame from the molded resin packages.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects, features and advantages of

the present invention will become more apparent from the following detailed description when read in conjunction with the accompanying drawings, in which:

Fig. 1A is a cross-sectional view of a semiconductor device of a conventional SSOP type;

Fig. 1B is a bottom view of the semiconductor device shown in Fig. 1A;

Fig. 1C is a top view of the semiconductor device shown in Fig. 1A;

Fig. 2 is a cross-sectional view of a semiconductor device of a conventional BGA type;

Fig. 3 is a cross-sectional view of a semiconductor device according to a first embodiment of the present invention;

Fig. 4 is a side view of a step of a method of producing the semiconductor device shown in Fig. 3;

Fig. 5 is a plan view of a lead frame used to produce semiconductor devices according to the first embodiment of the present invention;

Fig. 6 is a cross-sectional view showing another step of the method of producing the semiconductor device shown in Fig. 3;

Fig. 7 is a bottom view of a resin package observed when the step shown in Fig. 6 is completed;

Fig. 8 is a cross-sectional view of a semiconductor device according to a second embodiment of the present invention;

Fig. 9 is an enlarged perspective view of a resin projection used in the semiconductor device shown in Fig. 8;

Fig. 10 is an enlarged perspective view of an alternative of the resin projection used in the semiconductor device shown in Fig. 8;

Fig. 11 is a cross-sectional view showing a step of a method of producing the semiconductor device according to the second embodiment of the present invention;

Fig. 12 is a cross-sectional view showing another step of the method of producing the semiconductor device according to the second embodiment of the present invention;

Fig. 13 is a bottom view of a package after the step shown in Fig. 12 is completed;

Fig. 14 is a cross-sectional view of a semiconductor device according to a third embodiment of the present invention;

Fig. 15 is an enlarged perspective view of resin projections used in the semiconductor device according to the third embodiment of the present invention;

Fig. 16 is a side view showing a step of a method of producing the semiconductor device according to the third embodiment of the present invention;

Fig. 17 is a plan view of a lead frame used to produce semiconductor devices according to the third embodiment of the present invention;

Fig. 18 is a cross-sectional view showing another step of the method of producing the semiconductor device according to the third embodiment of the present invention;

Fig. 19 is a cross-sectional view of a semiconductor device according to a fourth embodiment of the present invention;

Fig. 20 is a side view showing a process of a method of producing the semiconductor device shown in Fig. 19;

Fig. 21 is a cross-sectional view of a semiconductor device according to a fifth embodiment of the present invention;

Fig. 22 is a cross-sectional view of a semiconductor device according to a sixth embodiment of the present invention;

Fig. 23 is a cross-sectional view showing a step of a method of producing the semiconductor device

shown in Fig. 22;

Fig. 24 is a cross-sectional view of a semiconductor device according to a seventh embodiment of the present invention;

Fig. 25 is a plan view of a lead frame used to produce a semiconductor device according to an eighth embodiment of the present invention;

Fig. 26 is a plan view of another lead frame used to produce the semiconductor device shown in Fig. 24;

Fig. 27 is a cross-sectional view showing a step of a method of producing the semiconductor device according to the eighth embodiment of the present invention;

Fig. 28 is a cross-sectional view of the semiconductor device according to the eighth embodiment of the present invention;

Fig. 29 is a cross-sectional view of a semiconductor device according to a ninth embodiment of the present invention;

Fig. 30 is a plan view of a lead frame used to produce semiconductor devices according to the ninth embodiment of the present invention;

Fig. 31 is a cross-sectional view of the lead frame shown in Fig. 30;

Fig. 32 is a cross-sectional view of a semiconductor device according to a tenth embodiment of the present invention;

Fig. 33 is a bottom view of the semiconductor device according to the tenth embodiment of the present invention;

Fig. 34 is a plan view of the semiconductor device according to the tenth embodiment of the present invention, in which inner parts thereof are seen through a resin package;

Fig. 35 is a cross-sectional view of a metallic film having a single-layer structure;

Fig. 36 is a cross-sectional view of a metallic film having a two-layer structure;

Fig. 37 is a cross-sectional view of a metallic film having a three-layer structure;

Fig. 38 is a cross-sectional view of a metallic film having a four-layer structure;

Fig. 39 is a cross-sectional view showing a resist forming step of a method of producing the semiconductor device according to the tenth embodiment of the present invention;

Fig. 40 is a cross-sectional view showing a resist pattern forming step of the method of producing the semiconductor device according to the tenth embodiment of the present invention;

Fig. 41 is a cross-sectional view showing an etching step of the method of producing the semiconductor device according to the tenth embodiment of the present invention;

Fig. 42A is a plan view for explaining power supply portions formed in a lead frame;

Fig. 42B is a cross-sectional view taken along a line A-A shown in Fig. 42A;

Fig. 43 is a plan view of a lead frame unit which can be used in the method of producing the semiconductor devices according to the tenth embodiment of the present invention;

Fig. 44 is a cross-sectional view showing a metallic film forming step of the method of producing the semiconductor device according to the tenth embodiment of the present invention;

Fig. 45 is a cross-sectional view of the completed lead frame;

Fig. 46 is a cross-sectional view showing a chip mounting step of the method of producing the semiconductor device according to the tenth embodiment of the present invention;

Fig. 47 is a cross-sectional view showing a

connecting step of the method of producing the semiconductor device according to the tenth embodiment of the present invention;

Fig. 48 is a cross-sectional view showing a variation of the connecting step shown in Fig. 47;

Fig. 49 is a plan view of a sealing step of the method of the semiconductor device according to the tenth embodiment of the present invention;

Fig. 50 is a cross-sectional view of the lead frame observed when the sealing step is completed;

Fig. 51A is a plan view of the lead frame observed when the sealing step is completed;

Fig. 51B is a side view of the lead frame observed when the sealing step is completed;

Fig. 52A is a plan view showing a tape arranging step of the method of the semiconductor device according to the tenth embodiment of the present invention;

Fig. 52B is a side view of the tape arranging step of the method of the semiconductor device according to the tenth embodiment of the present invention;

Fig. 53 is a cross-sectional view of a separating step of the method of the semiconductor device according to the tenth embodiment of the present invention;

Fig. 54A is a plan view of semiconductor devices observed when the sealing step is completed;

Fig. 54B is a side view of the semiconductor devices observed when the sealing step is completed;

Fig. 55A is a plan view showing a first variation of the sealing step of the method of producing the semiconductor device according to the tenth embodiment of the present invention;

Fig. 55B is a plan view showing a second variation of the sealing step of the method of

producing the semiconductor device according to the tenth embodiment of the present invention;

Fig. 55C is a plan view showing a third variation of the sealing step of the method of producing the semiconductor device according to the tenth embodiment of the present invention;

Fig. 56 is a plan view observed when the tape arranging step for the lead frame shown in Fig. 55A is completed;

Fig. 57A is a plan view showing a fourth variation of the sealing step of the method of producing the semiconductor device according to the tenth embodiment of the present invention;

Fig. 57B is a side view showing the fourth variation of the sealing step of the method of producing the semiconductor device according to the tenth embodiment of the present invention;

Fig. 58 is a cross-sectional view of the lead frame observed when the fourth variation shown in Figs. 57A and 57B is completed;

Fig. 59 is a cross-sectional view of another separation step of the method of producing the semiconductor device according to the tenth embodiment of the present invention;

Fig. 60 is a cross-sectional view of a semiconductor device according to an eleventh embodiment of the present invention;

Fig. 61 is a cross-sectional view showing a metallic base forming step of a method of producing the semiconductor device according to the eleventh embodiment of the present invention;

Fig. 62 is a cross-sectional view showing a resist forming step of the method of producing the semiconductor device according to the eleventh embodiment of the present invention;

Fig. 63 is a cross-sectional view showing a half-etching step of the method of producing the

semiconductor device according to the eleventh embodiment of the present invention;

Fig. 64 is a cross-sectional view showing a plating step of the method of producing the semiconductor device according to the eleventh embodiment of the present invention;

Fig. 65 is a cross-sectional view showing a resist removing step of the method of producing the semiconductor device according to the eleventh embodiment of the present invention;

Fig. 66 is a cross-sectional view showing a photosensitive resin coating step of the method of producing the semiconductor device according to the eleventh embodiment of the present invention;

Fig. 67 is a cross-sectional view showing a through hole forming step of the method of producing the semiconductor device according to the eleventh embodiment of the present invention;

Fig. 68 is a cross-sectional view showing a plating step of the method of producing the semiconductor device according to the eleventh embodiment of the present invention;

Fig. 69 is a cross-sectional view showing a resist forming step of the method of producing the semiconductor device according to the eleventh embodiment of the present invention;

Fig. 70 is a cross-sectional view showing etching and resist removing steps of the method of producing the semiconductor device according to the eleventh embodiment of the present invention;

Fig. 71 is a cross-sectional view of a semiconductor device according to a twelfth embodiment of the present invention;

Fig. 72 is a cross-sectional view showing a metallic base forming step of a method of producing the semiconductor device according to the twelfth embodiment of the present invention;

Fig. 73 is a cross-sectional view showing a resist forming step of the method of producing the semiconductor device according to the twelfth embodiment of the present invention;

Fig. 74 is a cross-sectional view showing a half-etching step of the method of producing the semiconductor device according to the twelfth embodiment of the present invention;

Fig. 75 is a cross-sectional view showing a half-etching step of the method of producing the semiconductor device according to the twelfth embodiment of the present invention;

Fig. 76 is a cross-sectional view showing a resist removing step of the method of producing the semiconductor device according to the twelfth embodiment of the present invention;

Fig. 77 is a cross-sectional view showing a photosensitive resin coating step of the method of producing the semiconductor device according to the twelfth embodiment of the present invention;

Fig. 78 is a cross-sectional view showing a window forming step of the method of producing the semiconductor device according to the twelfth embodiment of the present invention;

Fig. 79 is a cross-sectional view showing a plating step of the method of producing the semiconductor device according to the twelfth embodiment of the present invention;

Fig. 80 is a cross-sectional view showing a resist forming step of the method of producing the semiconductor device according to the twelfth embodiment of the present invention;

Fig. 81 is a cross-sectional view showing etching and resist separating steps of the method of producing the semiconductor device according to the twelfth embodiment of the present invention;

Fig. 82 is a cross-sectional view of a

semiconductor device according to a thirteenth embodiment of the present invention;

Fig. 83 is a cross-sectional view of a semiconductor device according to a fourteenth embodiment of the present invention;

Fig. 84A is a plan view of the semiconductor device shown in Fig. 83;

Fig. 84B is a side view of the semiconductor device shown in Fig. 83;

Fig. 84C is a bottom view of the semiconductor device shown in Fig. 83;

Fig. 85 is a cross-sectional view of the semiconductor device according to the fourteenth embodiment of the present invention in which the device is mounted to a circuit board;

Fig. 86 is a cross-sectional view of a metallic film having a five-layer structure;

Fig. 87 is a cross-sectional view of a metallic film having a six-layer structure;

Fig. 88 is a cross-sectional view of a metallic film having a seven-layer structure;

Figs. 89A, 89B, 89C, 89D and 89E are respectively cross-sectional views showing a variation of the connecting step;

Figs. 90A, 90B, 90C, 90D, 90E, 90F, 90G, 90H and 90I are respectively side views showing a method of forming stud bumps;

Fig. 91 is a cross-sectional view of a die used in the molding step;

Fig. 92 is a transverse-sectional view of an upper die of the die shown in Fig. 91;

Fig. 93 is a cross-sectional view of the lead frame observed when the sealing step is completed;

Fig. 94 is a side view showing a variation of the separating step;

Fig. 95 is a cross-sectional view showing

another variation of the separating step;

Fig. 96 is a cross-sectional view showing a through hole formed in the lead frame;

Fig. 97 is an enlarged perspective view of a through hole formed in a runner frame;

Fig. 98A and 98B are respectively enlarged plan views of through holes formed in runner frames;

Figs. 99A, 99B and 99C are respectively cross-sectional views showing still another variation of the separating step;

Fig. 100A is a side view showing separation grooves formed in the runner frames;

Fig. 100B is a plan view of the separation grooves shown in Fig. 100A;

Fig. 101 is an enlarged perspective view of a separation groove formed in the runner frame;

Figs. 102A, 102B, 102C, 102D and 102E are respectively cross-sectional views showing another separating step;

Figs. 103A and 103B are cross-sectional views showing a packaging step;

Fig. 104 is a cross-sectional view of a semiconductor device according to a fifteenth embodiment of the present invention;

Fig. 105 is a bottom view of a semiconductor device according to a sixteenth embodiment of the present invention;

Fig. 106 is a cross-sectional view of the semiconductor device shown in Fig. 105, in which the device is mounted on a circuit board;

Fig. 107 is a cross-sectional view of a semiconductor device according to a seventeenth embodiment of the present invention;

Fig. 108 is a bottom view of the semiconductor device shown in Fig. 107;

Fig. 109 is a plan view of the semiconductor device shown in Fig. 107 in which inner parts thereof

are seen through the package thereof;

Fig. 110 is a cross-sectional view of a semiconductor device according to an eighteenth embodiment of the present invention;

Fig. 111 is a bottom view of the semiconductor device shown in Fig. 110;

Fig. 112 is a cross-sectional view of semiconductor devices arranged on a circuit board according to the eighteenth embodiment of the present invention;

Fig. 113 is a cross-sectional view of an arrangement different from that shown in Fig. 112;

Fig. 114 is a cross-sectional view of an arrangement different from the arrangements shown in Figs. 112 and 113, in which semiconductor devices are inclined on the circuit board;

Fig. 115 is a cross-sectional view of the semiconductor device mounted on the circuit board according to the eighteenth embodiment of the present invention;

Fig. 116 is a cross-sectional view of a semiconductor device according to a nineteenth embodiment of the present invention;

Fig. 117 is a top view of the semiconductor device shown in Fig. 116, in which inner parts are seen through a resin package thereof;

Fig. 118 is a cross-sectional view of a metallic film having a single-layer structure;

Fig. 119 is a cross-sectional view of a metallic film having a two-layer structure;

Fig. 120 is a cross-sectional view of a metallic film having a three-layer structure;

Fig. 121 is a cross-sectional view of a metallic film having a four-layer structure;

Fig. 122 is a cross-sectional view showing a resist coating step of a method of producing the semiconductor device according to the nineteenth

embodiment of the present invention;

Fig. 123 is a cross-sectional view showing a resist pattern forming step of the method of producing the semiconductor device according to the nineteenth embodiment of the present invention;

Fig. 124 is a cross-sectional view showing a metallic film forming step of the method of producing the semiconductor device according to the nineteenth embodiment of the present invention;

Fig. 125 is a cross-sectional view of a completed lead frame;

Fig. 126 is a cross-sectional view showing a chip mounting step of the method of producing the semiconductor device according to the nineteenth embodiment of the present invention;

Fig. 127 is a cross-sectional view showing a connecting step of the method of producing the semiconductor device according to the nineteenth embodiment of the present invention;

Fig. 128 is a cross-sectional view showing a variation of the connecting step shown in Fig. 127;

Fig. 129 is a cross-sectional view of the lead frame observed when the sealing step is completed;

Fig. 130 is a cross-sectional view showing a separating step of the method of producing the semiconductor device according to the nineteenth embodiment of the present invention;

Fig. 131 is a cross-sectional view of a variation of the separating step shown in Fig. 130;

Fig. 132A is a cross-sectional view of a semiconductor device according to a twentieth embodiment of the present invention;

Fig. 132B is a top view of the semiconductor device shown in Fig. 132A in which inner parts are seen through a resin package thereof;

Fig. 133 is a cross-sectional view of a

semiconductor device according to a twenty-first embodiment of the present invention;

Fig. 134 is a cross-sectional view of a semiconductor device according to a twenty-second embodiment of the present invention;

Fig. 135 is a cross-sectional view of a semiconductor device according to a twenty-third embodiment of the present invention;

Fig. 136A is a cross-sectional view of a variation of the semiconductor device shown in Fig. 133, in which bumps as used in the device shown in Fig. 135 are employed;

Fig. 136B is a cross-sectional view of a variation of the structure shown in Fig. 136A;

Fig. 137 is a cross-sectional view of a variation of the semiconductor device shown in Fig. 134, in which bumps as used in the device shown in Fig. 135 are employed;

Fig. 138 is a cross-sectional view of a variation of the structure shown in Fig. 137;

Fig. 139A is a cross-sectional view of a semiconductor device in which a heat radiating member is attached to an exposed surface of a chip of the device shown in Fig. 138;

Fig. 139B is a cross-sectional view of a semiconductor device in which a heat radiating member having fins is attached to the exposed surface of the chip of the device shown in Fig. 138;

Fig. 140 is a cross-sectional view of a semiconductor device in which an insulating member is provided to the structure shown in Fig. 138; and

Figs. 141A, 141B and 141B are respectively cross-sectional views of a semiconductor device in which an anisotropically electrically conductive resin is employed.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 3 shows a semiconductor device according to a first embodiment of the present invention. The device shown in Fig. 3 includes a chip 11, electrode pads 12, bonding wires 13, a resin package 14, wire exposing portions 15, and solder balls 16. The chip 11 may be a semiconductor chip, a surface acoustic wave (SAW) chip, a multichip module or the like. In the specification, chips (including chips which will be described later) are semiconductor chips, and resin-packaged devices including the above chips are semiconductor devices. However, if an SAW chip is packaged, such a resin-packaged device should be called an SAW device or the like.

Ends of the bonding wires 13 are bonded to the electrode pads 12 provided on the chip 11 by a wire bonder, and the other ends of the bonding wires 13 are exposed in the wire exposing portions 15 formed on the bottom surface of the resin package 14. The diameter of the wire exposing portions 15 is greater than that of the bonding wires 13. The exposed ends of the bonding wires 13 are flush with the bottom surface of the resin package. The solder balls 16 are joined to the bonding wires 13 in the wire exposing portions 15 in which the ends of the wires 13 are exposed from the resin package 14.

The above structure does not require the inner leads and outer leads necessary for the SSOP, so that there is no need to provide a lead extending area in which the inner leads are arranged as well as an area occupied by the outer leads. Further, the structure shown in Fig. 3 does not need a mount base necessary for providing solder balls in the BGA type. Hence, the semiconductor device according to the first embodiment of the present invention needs a smaller mounting area and is less expensive.

A description will now be given of a method of producing the semiconductor device shown in Fig. 3.

As shown in Fig. 4, the chip 11 is mounted on a lead frame 17 by a die attaching agent 18. The lead frame 17 is made of an alloy such as a copper alloy, and is 0.1 - 0.2 mm thick. Next, the bonding wires 13 are bonded to the electrode pads 12 on the chip 11 and predetermined portions of the lead frame 17. The above predetermined portions are plated with Au, Ag, Pd or the like.

Then, as shown in Fig. 5, the lead frame 17 on which the chip 11 is mounted is accommodated in a die (not shown), and is then sealed by molding resin. In this step, the molded resin is provided up to an area indicated by mold lines 19 which enclose the wire exposing portions 15.

Thereafter, as shown in Fig. 6, the resin package 14 is separated from the lead frame 17. The separating step can be carried out by utilizing a process based on the difference between linear expansion coefficients of the resin package 14 and the lead frame 17, or another process in which the resin package 14 and the lead frame 17 are joined with a less-tight adhesiveness. For example, the surface of the lead frame 17 is plated or made to be flat. By the above process, the separating process can be facilitated.

Fig. 7 is a bottom view of the package after the separating process is carried out. The wire exposing portions 15 are located so as to surround the chip 11. The area of each of the wire exposing portions 15 is greater than the area of the cross section of each of the bonding wires 13 because the ends of the wires are crushed and shaped into a nail head shape during the bonding process.

The bonding may be carried out in the state shown in Fig. 7. Alternatively, the solder balls 16 can be provided to the wire exposing portions 15, as shown in Fig. 3. The solder balls 16 can be formed by

forming balls of solder (about $\phi 0.5$ - $\phi 0.8$) beforehand, placing the balls in the wire exposing portions 15 with a flux applied, and performing a reflow heat treatment, so that the spherically-shaped solder balls 16 can be formed.

[Second Embodiment]

A description will now be given, with reference to Figs. 8 through 13, of a semiconductor device and its production method according to a second embodiment of the present invention. In these figures, parts that are the same as those shown in the previously described figures are given the same reference numbers.

Fig. 8 shows a semiconductor device according to the second embodiment of the present invention, which has resin projections 21 projecting from the bottom surface (the mounting side) of the package by, for example, 0.05 - 1.00 mm. The bonding wires 13 are exposed from the bottom surfaces of the resin projections 21. The area of each of the wire exposing portions 15 is greater than the area of the cross-section of each of the bonding wires 13.

The resin projections 21 may have a rectangular parallelepiped shape as shown in Fig. 9, a cylindrical shape as shown in Fig. 10, or an arbitrary shape.

The solder balls 16 are joined to the wire exposing portions 15. Due to the resin projections 21, the solder balls 16 do not flush with the bottom surface of the package. This structure is not affected by a curvature or deformation of the package. Further, the above structure reduces the possibility of occurrence of a bridge of solder, which connects some solder balls.

The semiconductor device according to the second embodiment of the present invention can be

produced as follows.

As shown in Fig. 11, the chip 11 is mounted on the lead frame 17 by the die attaching agent 18. Next, the electrode pads provided on the chip 11 and recess portions 22 formed on the lead frame 17 are bonded together by the bonding wires 13. The bottom surfaces of the recess portions 22 formed on the lead frame 17 are plated in order to enable wire bonding.

Then, in the same manner as that of the first embodiment of the present invention, the lead frame 17 on which the chip 11 is mounted is accommodated in a die (not shown), and is then sealed by molding resin. In this process, the resin is molded up to the area which encloses the wire exposing portions 15, as in the case of the first embodiment of the present invention.

Thereafter, as shown in Fig. 12, the resin package 14 is separated from the lead frame 17 in the same manner as that of the first embodiment of the present invention.

Fig. 13 shows a bottom view of the package after the separating process is carried out. The wire exposing portions 15 in the resin projections 15 are located so as to surround the chip 11. The area of each of the wire exposing portions 15 is greater than the area of the cross section of each of the bonding wires 13.

In the state shown in Fig. 13, solder paste may be coated to lands provided on a circuit board, and then the package may be mounted on the circuit board. Alternatively, solder balls 16 shown in Fig. 8 may be provided to the wire exposing portions 15. The solder balls 16 can be formed in the same manner as those used in the first embodiment of the present invention.

[Third Embodiment]

A description will now be given, with reference to Figs. 14 through 18, of a semiconductor device according to a third embodiment of the present invention and its production method. In these figures, parts that are the same as those shown in the previously described figures are given the same reference numbers.

Fig. 14 shows a semiconductor device according to the third embodiment of the present invention, which has recess portions 23 formed in the resin package 14 and solder-buried portions 24. The solder balls 16 are connected to the bonding wires 13 via the solder-buried portions 24.

Fig. 15 shows a package observed before the solder balls 16 are provided and the solder-buried portions 24 are formed. The bottoms of the recess portions 23 are 0.05 - 0.20 mm lower than the bottom surface of the package. The ends of the bonding wires 13 are exposed in the bottoms of the recess portions 23. The area of each of the wire exposing portions is greater than the area of the cross section of each of the bonding wires 13. The recess portions 23 may have a rectangular parallelepiped shape, a cylindrical shape or an arbitrary shape.

The solder-buried portions 24 are provided between the solder balls 16 and the wire exposing portions 15. Due to the solder-buried portions 24, the strength of joining the solder balls 16 and the wire exposing portions 15 can be enhanced as compared with those in the first and second embodiments of the present invention. This is because larger end portions 13c of the bonding wires 13 can be joined to the solder-buried portions 24, and the solder balls 16 can be joined to the entire exposed surfaces of the solder-buried portions 24.

A method of producing the semiconductor device shown in Fig. 14 will be described below.

As shown in Fig. 16, the chip 11 is mounted on the lead frame 17 by the dice attaching agent 18. Next, the electrode pads provided on the chip 11 and protruding portions 25 formed on the lead frame 17 are bonded together by the bonding wires 13. The protruding portions 25 formed on the lead frame 17 are plated in order to enable wire bonding.

A half-etching step is carried out for the lead frame 17, as shown by oblique lines shown in Fig. 17 except for the protruding portions 25 in order to define the protruding portions 25. Alternatively, a stamping process can be used to form the protruding portions 25. In the stamping process, punches are provided to terminal forming areas and the lead frame 17 is plastically deformed

Then, in the same manner as that of the first embodiment of the present invention, the lead frame 17 on which the chip 11 is mounted is accommodated in a die (not shown), and is then sealed by molding resin. In this process, the molded resin extends up to the area which encloses the wire exposing portions 15, as in the case of the first embodiment of the present invention.

Thereafter, as shown in Fig. 18, the resin package 14 is separated from the lead frame 17 in the same manner as that of the first embodiment of the present invention.

Fig. 13 shows a bottom view of the package after the separating process is carried out. it will be noted that Fig. 13 was used in the aforementioned description directed to the second embodiment of the present invention. It will be noted that the recess and protruding portions cannot be discriminated in the bottom views of the packages used in the second and third embodiments. The wire exposing portions 15 exposed in the recess portions 23 are located so as to surround the chip 11. The area of each of the wire

exposing portions 15 is greater than the area of the cross section of each of the bonding wires, as in the case of the first embodiment of the present invention.

The solder balls 16 provided to the wire exposing portions 15 shown in Fig. 14 are needed to mount the semiconductor device on a circuit board. The solder balls 16 can be formed by directly placing solder balls in the recess portions 23 and forming them into a spherical shape after the reflow heat treatment. In this step, solder is provided in the solder-buried portions 24. Alternatively, solder paste can be buried in the solder-buried portions 24 by a screen printing process, and solder balls are given thereto and heated so that the solder balls are shaped in a sphere.

[Fourth Embodiment]

A description will now be given, with reference to Figs. 19 and 20, of a semiconductor device according to a fourth embodiment of the present invention. In these figures, parts that are the same as those shown in the previously described figures are given the same reference numbers.

The fourth embodiment of the present invention differs from the first embodiment thereof in that bonding balls (bumps) 26 are provided between the ends of the bonding wires 13 and the solder balls 16. The area of each of the wire exposing portions 15 is greater than the area of the cross-section of each of the bonding wires 13. Hence, it is possible to make a more reliable contact between the bonding wires 13 and the solder balls 16.

The device shown in Fig. 19 is produced as follows. Referring to Fig. 20, the chip 11 is mounted on the lead frame 17, and then the bonding wires 13 are bonded, by means of a wire bonder, to electrode pads provided on the chip 11 and the bonding balls 26

provided on the lead frame 17. The bonding balls 26 are provided in given positions on the lead frame 17 after the chip 11 is mounted on the lead frame 17 and before the bonding wires 13 are bonded.

Then, in the same manner as that of the first embodiment of the present invention, the lead frame 17 on which the chip 11 is mounted is accommodated in a die (not shown), and is then sealed by molding resin. Thereafter, the resin package 14 is separated from the lead frame 17 in the same manner as that of the first embodiment of the present invention. In this state, the device may be mounted on a circuit board. Alternatively, the solder balls 16 may be provided to the wire exposing portions 15, as shown in Fig. 19. The solder balls 16 can be formed in the same manner as those of the first embodiment of the present invention.

[Fifth Embodiment]

A description will now be given, with reference to Fig. 21, of a semiconductor device according to a fifth embodiment of the present invention. The semiconductor device shown in Fig. 21 corresponds to a combination of the second embodiment of the present invention shown in Fig. 8 and the fourth embodiment thereof shown in Fig. 19. In Fig. 21, parts that are the same as those shown in the previously described figures are given the same reference numbers.

The fifth embodiment of the present invention has a feature such that the bonding balls 26 are exposed from the bottom surfaces of the resin projections 21, and the solder balls 16 are connected to the exposed bonding balls 26. This structure is not affected by a curvature of the package. Further, the above structure reduces the possibility of occurrence of a bridge of solder, which connects some

solder balls. Furthermore, the bonding balls 26 are greater than the ends of the bonding wires 13, so that a more reliable contact can be made when mounting the device on a circuit board.

[Sixth Embodiment]

A description will now be given, with reference to Figs. 22 and 23, of a semiconductor device according to a sixth embodiment of the present invention. In these figures, parts that are the same as those shown in the previously described figures are given the same reference numbers.

The sixth embodiment of the present invention has a feature such that bonding balls 27 as shown in Fig. 22 serving as terminals for mounting are provided instead of the above-mentioned solder balls 16. Each of the bonding balls 27 has a projection projecting from the bottom surface of the resin package 14. The length of the projection is, for example, tens of microns. Hence, the bonding balls 27 do not need any solder balls like the solder balls 16. That is, the bonding balls 27 can be directly mounted to a circuit board.

The semiconductor device shown in Fig. 22 can be produced as follows.

Referring to Fig. 23, the chip 11 is mounted on the lead frame 17 by the die attaching agent 18, as in the case of the first through fifth embodiments of the present invention. Next, the bonding wires 13 are bonded to the electrode pads provided on the chip 11 and recess portions 28 formed on the lead frame 17. The diameter of the recess portions 28 is less than that of the bonding balls 27. When the bonding balls 27 are pressed against the recess portions 28, the bonding balls 27 are partially inserted into the recess portions 28, so that the relationship between the bonding balls 27 and the recess portions 28 is as

shown in Fig. 23. The bottom surfaces of the recess portions 28 formed in the lead frame 17 are plated in order to enable wire bonding.

Then, in the same manner as that of the first embodiment of the present invention, the lead frame 17 on which the chip 11 is mounted is accommodated in a die (not shown), and is then sealed by molding resin. Thereafter, the resin package 14 is separated from the lead frame 17 in the same manner as that of the first embodiment of the present invention.

[Seventh Embodiment]

A description will now be given, with reference to Fig. 24, of a semiconductor device according to a seventh embodiment of the present invention, which has almost the same structure as that of the third embodiment thereof except that the device shown in Fig. 24 employs bonding balls 29.

As shown in Fig. 24, the solder balls 16 are connected to the bonding wires 13 through the solder-buried portions 24. Further, the bonding balls 29 are provided between the solder-buried portions 24 and the bonding wires 13. The bonding balls 29 are greater in size than the ends of the bonding wires 13, so that the reliability of making a contact can be increased. Further, due to the solder-buried portions 24, the strength of joining the solder balls 16 thereto can be enhanced.

[Eighth Embodiment]

A description will now be given, with reference to Figs. 25 through 28, of a semiconductor device and its production method according to an eighth embodiment of the present invention. In the above-mentioned first through seventh embodiments of the present invention, the chip 11 is exposed in the bottom surface of the resin package 14. In the eighth

embodiment of the present invention, the chip 11 is mounted on a die stage 32, which is exposed in the bottom surface of the resin package 14, as shown in Figs. 26 and 28.

The semiconductor device shown in Fig. 28 can be produced as follows.

The chip is mounted on the die stage 32 of a lead frame 31 by a die attaching agent. Next, the lead frame 31 is stacked on a lead frame 30, and is fixed thereto by spot welding. Then, the bonding wires 13 are bonded to electrode pads on the chip 11 and given positions on the lead frame 30. The given positions of the lead frame 30 or the entire lead frame 30 is plated in order to enable wire bonding.

As shown in Fig. 25, the lead frames 30 and 31 are accommodated in a die (not shown), and are then sealed by molding resin. In this process, the molded resin extends up to the area which encloses the wire exposing portions 15. Thereafter, only the lead frame 30 is mechanically separated from the resin package 14. Then, the solder balls 16 are provided as in the case of the first embodiment of the present invention.

[Ninth Embodiment]

A description will now be given, with reference to Figs. 29 through 31, of a semiconductor device and its production method according to a ninth embodiment of the present invention. In these figures, parts that are the same as those shown in the previously described figures are given the same reference numbers.

As shown in Fig. 29, first balls 35 are formed by bonding solder wires 34 mainly containing Pb-Sn to the electrode pads 12 on the chip 11. The solder wires 34 penetrate through a lead frame 33, and form second balls 36 on the surface of the lead frame 33 opposite to the surface thereof on which the chip

11 is mounted.

The mounting of the semiconductor device shown in Fig. 29 on a circuit board is completed by soldering the second balls 36 to a foot print on the circuit board. Since the ends of the solder wires 34 form the second balls 36 for electrical connections to the circuit board, the wire bonding process and the process for forming the terminals for electrical connections to the circuit board are simultaneously carried out.

The semiconductor device shown in Fig. 29 can be produced as follows.

As shown in Fig. 30, a half-etching process is carried out so that the central portion of the lead frame 33 is half-etched so that the peripheral portion of each die stage remains. Hence, a half-etched area 37 is formed. The lead frame 33 has through holes 38, as shown in Figs. 30 and 31. Next, the chip 11 is mounted on the die stage of the lead frame 33 by a dice attaching agent.

Then, the solder wires 34 first are bonded to the electrode pads 12 on the chip 11, and second are bonded to the given positions on the lead frame 33. In the second bonding process, the solder balls formed by a spark are pushed against the through holes 38 by means of an end of a capillary (not shown), so that the solder balls are pushed out of the through holes 38. Hence, the second balls 36 are formed on the surface of the lead frame 33 opposite to its chip mounting surface.

Thereafter, the lead frame 33 on which the chip 11 is mounted is accommodated in a die, and is then sealed by molding resin. In this process, the molded resin extends up to the area which surrounds the second balls 36. Then, the resin package 14 is separated from the lead frame 33.

[Tenth Embodiment]

A description will now be given of a semiconductor device and its production method according to a tenth embodiment of the present invention.

Fig. 32 is a cross-sectional view of a semiconductor device 110 according to the tenth embodiment of the present invention, and Fig. 33 is a bottom view of the semiconductor device 110. Fig. 34 is a plan view of the semiconductor device 110 seen through a resin package 112 which will be described later.

The semiconductor device 110 is mainly made up of a chip 111, a resin package 112 and metallic films 113. A plurality of electrode pads 114 are provided on the upper surface of the chip 111, which is mounted on a chip fixing resin 115. The chip 111 may be a semiconductor chip, a SAW chip, a multichip module or the like.

The resin package 112 is formed by molding epoxy resin or the like, as will be described later. A potting can be used to form the resin package 112. Resin projections 117, which are integrally formed with the resin package 112, are located in given positions on the bottom surface (mounting-side surface) of the resin package 112. The resin projections 117 are arranged at a pitch equal to, for example, 0.8 mm.

The metallic films 113 are provided so that they respectively cover the resin projections 117. Bonding wires 118 are provided between the metallic films 113 and the electrode pads 114, so that the metallic film 113 and the chip 111 are electrically connected together. Bonding balls 101 like the aforementioned bonding balls 26 are provided in order to improve the bondability of the bonding wire 118 to the metallic film 113. The details of the metallic

films 113 will be described later.

The semiconductor device 110 thus formed does not need any inner and outer leads used in the SSOP. Hence, there is no need to provide an area for leading the inner leads and a space in which the outer leads extend. Hence, a down-sized semiconductor device can be provided. Further, the semiconductor device 110 does not need any solder balls used in the BGA type, and is thus less expensive. Furthermore, the resin projections 117 and the metallic films 113 cooperate with each other as if they function as solder bumps of the BGA-type devices, so that a high mounting density can be obtained. Furthermore, the semiconductor device 110 is not affected by a curvature or deformation of the resin package 112.

A description will now be given, with reference to Figs. 35 through 38, of the metallic films 113. These figures are enlarged views of one of the metallic films 113.

As described above, the metallic film 113 covers the resin projection 117 and is electrically connected to the chip 111 by the bonding wire 118. The metallic film 113 functions as a terminal for an external connection, and is connected to an electrode part formed on a circuit board by soldering.

The metallic film 113 can be formed of a single metallic layer or a plurality of metallic layers stacked. Fig. 35 shows a metallic film 113A, which is formed of a single metallic layer, and Figs. 36 through 38 respectively show metallic films 113B, 113C and 113D formed of a plurality of metallic layers.

A substance or substances of the metallic films 113 (113A - 113D) should be selected taking into account the following. The inner portion of the metallic film 113 is to be bonded to the bonding wire 118, and the outer portion thereof is to be soldered

to an electrode on the circuit board. Hence, it is required that the inner portion (the innermost layer) of the metallic film 113 has a good bondability and the outer portion (the outermost layer) thereof has a good ability of soldering. The above requirement (hereinafter referred to as a film requirement) can be satisfied by the following substances.

It is required that a substance of the metallic film 113A shown in Fig. 35 has both a good bondability and a good ability of soldering. Such a material is, for example, silver (Ag) or palladium (Pd).

The metallic film 113B shown in Fig. 36 is made up of an outer layer 113B-1 and an inner layer 113B-2. By way of example, the outer layer 113B-1 can be made of palladium (Pd), and the inner layer 113B-2 can be made of gold (Au) so that the film requirement can be satisfied.

The metallic film 113C shown in Fig. 37 is made up of an outer layer 113C-1, an intermediate layer 113C-2 and an inner layer 113C-3. By way of example, the outer layer 113C-1 can be made up of gold (Au), the intermediate layer 113C-2 can be made up of nickel (Ni), and the inner layer 113C-3 can be made up of gold (Au) so that the film requirement can be satisfied.

Alternatively, the following combinations can be employed.

113C-1	113C-2	113C-3
palladium (Pd)	nickel (Ni)	palladium (Pd)
gold (Au)	palladium (Pd)	gold (Au)
solder	nickel (Ni)	gold (Au)
solder	nickel (Ni)	palladium (Pd)

The above combinations satisfy the film requirement and improve the ability of joining the

outer layer 113C-1 and the inner layer 113C-3 due to the intermediate layer 113C-2.

The metallic film 113D shown in Fig. 38 is made up of an outer layer 113D-1, a first intermediate layer 113D-2, a second intermediate layer 113D-3 and an inner layer 113D-4. These layers can be formed by the following substances.

113D-1	113D-2	113D-3	113D-4
solder	nickel (Ni)	palladium (Pd)	gold (Au)
palladium (Pd)	nickel (Ni)	palladium (Pd)	gold (Au)

The above combinations satisfy the film requirement and improve the ability of joining the outer layer 113D-1 and the inner layer 113D-4 due to the intermediate layers 113D-2 and 113D-3.

A description will now be given of a method of producing the semiconductor device 110 according to the tenth embodiment of the present invention. By way of example, the following description is directed to forming the semiconductor device 110 equipped with the three-layer structure metallic film 113C made up of the outer layer 113C-1, the intermediate layer 113C-2 and the inner layer 113C-3.

The semiconductor device 110 is produced by using a lead frame 120 shown in Fig. 45. The lead frame 120 has an electrically conductive metallic member 121 having a plurality of recess portions 122. The metallic films 113C are respectively provided in the recess portions 122. The recess portions 122 are positioned so that they correspond to the positions in which the resin projections 117 should be formed. The metallic films 113C are formed so as to engage the resin projections 117.

As will be described later, the lead frame 120 is configured so that a plurality of semiconductor devices 110 can be produced. Hence, the metallic

member 121 has the plurality of recess portions 122 and the plurality of metallic films 113C, as shown in Fig. 42A, in which a reference number 123 indicates tool engagement holes with which a tool for handling the lead frame 120 engages.

Before describing the method of producing the semiconductor device 110, a description will first be given, with reference to Figs. 39 through 45, of a method of producing the lead frame 120.

As shown in Fig. 39, the plate-shaped metallic member 121 made of an electrically conductive material such as copper is prepared. Etching resist films 124 are provided on the upper and lower surfaces of the metallic member 121 (resist coating step). The etching resist films 124 are made of a photosensitive resin, and are provided to a given thickness by means of a spinner. Alternatively, it is possible to use a metallic member in which the tool engagement holes 123 are formed by stamping or the like before the etching resist films 124 are provided.

Then, an exposure step is carried out by using masks (not shown) formed on the etching resist films 124. Subsequently, a developing step is carried out so that portions of the etching resist films 124 corresponding to the positions of the recess portions 122 and the tool engagement holes 123 are removed. Hence, resist patterns 124a are formed, as shown in Fig. 40 (resist pattern forming step). In the resist pattern forming step, portions of the etching resist films 124 in which power supply portions 125 (Figs. 42A and 42B) should be formed are removed. The power supply portions 125 are plated in a metallic film forming step which will be described later. If the above alternative metallic member is used, there is no need to form windows therein directed to forming the tool engagement holes 123.

Subsequent to the above resist pattern

forming step, the metallic member 121 on which the resist patterns 124a are formed is etched (etching step). In the etching step, portions of the metallic member 121 corresponding to the recess portions 122 and the power supply portions 125 are half-etched from the upper surface thereof. Further, portions of the metallic member 121 corresponding to the tool engagement holes 123 are etched from the upper and lower surfaces of the metallic member 121. When the metallic member 121 is made of copper, an etchant used in the etching step is, for example, ferric chloride.

Hence, as shown in Fig. 41, the recess portions 122 and the tool engagement holes 123 are formed in given positions of the metallic member 121. As shown in Figs. 42A and 42B, the power supply portions 125 are formed in the metallic member 121. The depth of the recess portions 122 defined by the half-etching process is made equal to 60% of the thickness of the metallic member 121.

The power supply portions 125 are located in end portions of the metallic member 121 in the longitudinal direction thereof. In the power supply portions 125, the metallic member 121 is exposed. Hence, by plating the power supply portions 125, the metallic member 121 can be set to a given potential. It will be noted that Fig. 42B is a cross-sectional view taken along a line A-A shown in Fig. 42A.

In Fig. 42A, blocks depicted by broken lines respectively denote positions in which the semiconductor devices 110 are formed. In the metallic member 121 shown in Fig. 42A, 34 semiconductor devices 110 can be derived therefrom. A plurality of recess portions 122 are formed for each of the plurality of semiconductor devices 110.

In order to form more semiconductor devices 110 from a single metallic member, a lead frame unit 128 as shown in Fig. 43 can be used. The lead frame

unit 128 has a frame 126, and a plurality of metallic members 121 joined to the frame 126 by means of joint portions 127 provided on two opposite sides of each of the metallic members 121 in the longitudinal direction thereof. It is necessary to form power supply portions 125 in the lead frame unit 128. The power supply portions 125 can be formed in the frame 126 so that electricity can be supplied to all the metallic members 121 via the joint portions 127.

The use of the lead frame unit 128 contributes to improving the efficiency of the method of producing the semiconductor devices 110. Further, as compared to the structure shown in Fig. 42A, a simplified resist pattern forming step and a simplified etching step can be employed.

After the etching step, the metallic film forming step which has been briefly referred to is carried out in order to form the metallic film 113C. In the tenth embodiment of the present invention, the metallic film 113C is formed by plating. For example, electrolytic plating can be employed in which the metallic member 121 is placed in a plating chamber. In this step, the aforementioned power supply portions 125 are concurrently plated.

Since the metallic film 113C is made up of the outer layer 113C-1, the intermediate layer 113C-2 and the inner layer 113C-3, the plating step is carried out for each of these three layers. If the outer layer 113C-1, the intermediate layer 113C-2 and the inner layer 113C-3 are respectively formed of gold (Au), palladium (Pd) and gold (Au), the plating step commences with plating of the inner layer 113C-1 with gold. Next, the intermediate layer 113C-2 is plated with palladium (Pd), and then the outer layer 113C-3 is plated with gold (Au). The thickness of each of the layers 113C-1 through 113C-3 can be regulated by controlling the plating time. Fig. 44 shows the

metallic member 121 on which the metallic films 113C are formed.

As will be described in detail later, it is necessary to separate the metallic films 113C together with the resin package 112 from the lead frame 120. Hence, it is required that the metallic films 113C have a nature which enables the metallic films 113C to be smoothly separated from the metallic member 121. With the above in mind, a material which facilitates the separating process, such as an electrically conductive paste, is provided in the recess portions 122 before the metallic films 113C are formed therein. Hence, the metallic films 113C are formed on the above material.

It should be noted that the metallic films 113C can be formed by thin-film forming processes other than the plating process, such as an evaporating process and a sputtering process.

In addition to the recess portions 122, the metallic member 121 is exposed in the tool engagement holes 123, so that a film having the same structure as that of the metallic film 113C is formed in each of the tool engagement portions 123 in the metallic film plating step. However, there is no problem because the tool engagement portions 123 are specifically directed to being engaged with the tool and used to position and handle the metallic member 121.

Then, a resist removing step is carried out in order to remove the resist patterns 124a (etching resist films 124). Hence, the lead frame 120 shown in Fig. 45 is formed. As described above, the lead frame 120 can be formed by a simple sequence including the resist coating step, the resist pattern forming step, the etching step, the metallic film forming step and the resist removing step.

A description will now be given, with reference to Figs. 46 through 59, of a method of

producing the semiconductor device 110 using the lead frame 120 produced in the above-mentioned process.

As shown in Fig. 46, a chip fixing resin 115 is provided on a portion of the lead frame 120 on which the chip 111 should be placed. Then, the chip 111 is mounted on the chip fixing resin 115 (chip mounting step). The chip fixing resin 115 has insulation, and functions as an adhesive. Thus, the chip 111 is fixed to the lead frame 120 by adhesive force of the chip fixing resin 115.

After the chip mounting step, the lead frame 120 is loaded to a wire bonding apparatus. As shown in Fig. 47, the bonding wires 118 are provided between the electrode pads 114 provided on the chip 111 and the metallic films 113C (more particularly, the inner layer 113C-3). Hence, the chip 111 and the metallic films 113C are electrically connected together. In the wire bonding step, the ends of the bonding wires 118 are bonded to the electrode pads 114 first (first bonding step), and the other ends thereof are bonded to the metallic films 113C.

Alternatively, as shown in Fig. 48, the ends of the wires 118 are bonded to the metallic films 113C first, and the other ends thereof are bonded to the electrode pads 114 second. This alternative makes it possible to reduce the height of the bonding wires 118. This leads to a reduction in the thickness of the semiconductor device 110.

Further, the aforementioned bonding balls 101 as shown in Fig. 32 can be employed. In this case, the bonding wires 118 are bonded to the bonding balls 101.

The electrode pads 114 are arranged at a pitch less than that at which the metallic films 113C are arranged. Further, the area in which the first bonding is carried out is greater than the area in which the second bonding is carried out. Hence, it is

possible to arrange the bonding wires 118 at a high density by performing the first bonding to the metallic films 113C first and the second bonding to the electrode pads 114 second.

After the bonding step, a sealing step is carried out so that a resin 129 is formed on the lead frame 120 so as to seal the chip 111 and thus form the resin package 112. In the following description, the resin package 112 is formed by molding. Alternatively, a potting process can be employed.

Fig. 49 schematically shows the state observed immediately after the lead frame 120 is loaded to a die and the resin 129 is molded. In Fig. 49, a reference number 130 indicates a curl, a reference number 131 indicates a runner, and a reference number 132 indicates a gate. As shown in Fig. 49, a plurality of resin packages 112 are formed on the lead frame 120. In the state immediately after the sealing step, the resin packages 112 are joined via portions of the resin 129 located on the gates 132. Hereinafter, such resin portions are referred to as on-gate resin portions.

Fig. 50 is an enlarged cross-sectional view of one of the resin packages 112 corresponding to one semiconductor device 110. As shown in Fig. 50, the resin 129 is formed in a given shape by a cavity (not shown) of a die (upper die), while the lead frame 120 functions as a lower die. The resin 129 is filled in the recess portions 122 (more particularly, recesses respectively defined by the metallic films 113C), so that the aforementioned resin projections 117, which are counterparts of the recess portions 122, are formed. In this state, the resin package 112 is impregnated to the lead frame 120.

After the resin packages 112 are formed, the on-gate resin, resin remaining in the runner 131 and the curl 130 are removed. Hence, as shown in Figs.

51A and 51B, the resin packages 112 are separated from each other on the lead frame 120. As described above, the resin packages 112 are impregnated to the lead frame 120 and thus are not detached from the lead frame 120 even if the resin packages 112 are separated from each other.

Subsequent to the sealing step, a tape arranging step is carried out. In this step, as shown in Figs. 52A and 52B, a tape member 133 is arranged on the tops of the resin packages 112. The tape member 133 has a surface coated with an adhesive, and a base tape which cannot be damaged by an etchant used in a separating step which will be carried out later. The tape member 133 joins the resin packages 112 together, so that the resin packages 112 are supported by the tape member 133 even when the resin packages 112 are separated from the lead frame 120.

The tape member 133 can be arranged at an appropriate time before the resin packages 112 are formed. For example, the tape member 133 can be arranged within the die prior to the sealing step. In this case, when the resin packages 112 are formed, the resin packages 112 are joined together by the tape member 133.

Following the tape arranging step, a separating step is carried out in order to separate the resin packages 112 from the lead frame 120. Fig. 53 shows the separating step, in which the lead frame 120 is placed in the etchant and is thus dissolved. It is required that the etchant used in the separating step can dissolve the lead frame 120 only and does not dissolve the metallic films 113C. When the lead frame 120 is completely dissolved, the resin packages 112 are separated from the lead frame 120. The above separating step makes it possible to certainly and easily separate the resin packages 112 from the lead frame 120.

Figs. 54A and 54B show the semiconductor devices 110 when the separating step is completed. At this time, the semiconductor devices 110 are supported by the tape member 133. Hence, it is easy to handle the chips 110 after the separation step. When the tape member 133 is wound and shipped, it is possible to automatically mount the semiconductor devices 110 to a circuit board, as in the case of chips or electronic components.

The above-mentioned production method does not need a lead cutting step and lead shaping step (into a gull wing) necessary for the conventional production process, and is therefore simple.

A description will now be given of variations of the above-mentioned method of producing the semiconductor device 110.

Fig. 55A shows a first variation of the sealing step. In the above-mentioned method, the resin packages 112 are joined by the on-gate resin portions as has been described with reference to Fig. 49. The on-gate resin portions are removed as shown in Figs 51A and 51B, and the tape member 133 is arranged as shown in Figs. 52A and 52B. As has been described, the tape member 133 is used to maintain the separated resin packages 112 in the respective original positions.

In the first variation, the on-gate resin portions and the resin 129 remaining in the runner 131 are used, instead of the tape member 133, as resin joint members joining the resin packages 112 together. Hereinafter, such resin joint members are referred to as a runner frame 134. Hence, it is possible to efficiently utilize the on-gate resin portions and the resin 129 remaining in the runner 131. The runner frame 134 should be removed when shipping the semiconductor devices 110. In this case, before shipping, the tape member 133 is provided as shown in

Fig. 56, and the runner frame 134 is removed (resin joint member removing step).

It is possible to prevent the tape member 133 from being damaged in the separating step and a step of testing the semiconductor devices 110 by providing the tape member 133 before shipping. This is advantageous when the semiconductor devices 110 are shipped in the state in which the devices 110 are shipped.

Fig. 55B shows a variation of the sealing step shown in Fig. 55A, in which the runner frames 134 extend laterally and longitudinally.

Fig. 55C shows another variation of the sealing step shown in Fig. 55A, in which the resin frames 112 are laterally and longitudinally supported by the runner frames 134. The resin to be removed can be efficiently utilized as the on-gate resin portions and the runner frames.

Figs. 57A, 57B and 58 show a fourth variation of the sealing step. In the aforementioned tenth embodiment of the present invention, the resin packages 112 are separated from each other when the sealing step is completed. In the fourth variation, the resin packages 112 are joined together when the sealing step is completed.

Figs. 57A and 57B show the lead frame 120 when the sealing step is completed in the fourth variation. As shown in these figures, the resin packages 112 are joined like a plate-shaped chocolate. There are grooves 135 at the boundaries of the adjacent resin packages 112. Hence, it is possible to keep the original positions of the resin packages 112 without the tape member 133. The resin packages 112 can be separated from each other in the grooves 135, which facilitate the separating step.

Fig. 58 shows a die 136 used to form the resin packages 112 shown in Figs. 57A and 57B. As

shown in Fig. 58, an upper die of the die 136 has a cavity in which projections 138 corresponding to the grooves 135 are formed. A lower die 139 of the die 136 has a recess portion 140 in which the lead frame 120 is placed. The resin packages 112 joined together as shown in Figs. 57A and 57B can be formed by using the die 136 having a simple structure.

Fig. 59 shows a variation of the separating step. The above-mentioned separating step employs etching. Instead, the variation is intended to mechanically separate the resin packages 112 from the lead frame 120 rather than dissolving the lead frame 20. The variation does not need any etchant and a smaller amount of time is necessary for the separation step. On the other hand, it should be considered whether the mechanical separating process certainly allows the metallic films 113C to move to the resin projections 117. The above possibility will be eliminated by providing a member which facilitates the mechanical separating process in the recess portions 122 beforehand.

[Eleventh Embodiment]

A description will now be given of a semiconductor device according to an eleventh embodiment of the present invention.

Fig. 60 shows a semiconductor device 150 according to the eleventh embodiment of the present invention. In this figure, parts that are the same as those shown in the previously described figures relating to the semiconductor device 110 are given the same reference numbers.

The semiconductor device 150 has a feature in which it has a resin package 151 having a two-layer structure made up of a upper resin layer 152 and a lower resin layer 153. A plurality of resin projections 154 are formed in given positions of the

lower resin layer 153. Metallic films 155 each having a single-layer structure made of, for example, palladium (Pd) respectively cover the resin projections 154.

Connection electrodes 156 are provided to the lower resin layer 153, and have lower extending portions 162 extending through through holes 157 formed in the lower resin layer 153. The ends of the lower extending portions 162 are electrically connected to the corresponding metallic films 155. The connection electrodes 156 respectively have upper bonding portions 163 located on the lower resin layer 153. The bonding wires 118 are bonded to the upper bonding portions 163.

The upper resin layer 152 and the lower resin layer 153 can be made of an identical substance or different substances. For example, the lower resin layer 153 on which the chip 111 is mounted is made of a resin having a good heat resistance and a good mechanical strength. The upper resin layer 152 is made of a resin having a good heat radiating nature. Hence, the characteristic of the chip 111 can be improved.

It is possible to employ a resin package consisting of three resin layers or more.

A description will now be given, with reference to Figs. 61 through 70, of a method of producing the semiconductor device 150 according to the eleventh embodiment of the present invention. The method of producing the semiconductor device 150 has a step of forming the metallic films 155 and the connection electrodes 156 which is not used in the method of producing the semiconductor device 110. The steps of producing the other portions of the semiconductor device 150 can be the same as corresponding ones of the step of producing the semiconductor device 110. Hence, the following

description will be focused on the step of producing the metallic films 155 and the connection electrodes 156.

As shown in Fig. 61, the plate-shaped metallic member 121 made of copper (Cu) or the like is prepared. An etching resist film made of a photosensitive resin is provided on the upper and lower surfaces of the metallic member 121 (resist coating step). Then, an exposure process is carried out using masks provided to the etching resist films. Thereafter, a developing process is carried out in order to remove portions of the etching resist films corresponding to the recess portions. Hence, the resist patterns 124a shown in Fig. 62 can be obtained (resist pattern forming step).

After the resist pattern forming step, the metallic member 121 on which the resist patterns 124a are formed is etched (etching step). In the etching step, the metallic member 121 is half-etched from only the upper surface thereof. Hence, as shown in Fig. 63, which is an enlarged view of a part B shown in Fig. 62, a recess portion 158 is formed in the recess forming portion defined by the upper resist pattern 124a.

The etching step is followed by a metallic film forming step in which the metallic films 155 are formed by plating. The metallic member 121 is placed in the plating chamber and electrolytic plating is carried out. Each of the metallic films 155 used in the embodiment of the present invention being considered has a palladium (Pd) single-layer structure. Hence, the metallic films 155 can be formed by performing the plating step once. Fig. 64 shows the metallic member 121 with the metallic film 155 plated in the recess portion 158.

It should be noted that the metallic films 155 can be formed by thin-film forming processes other

than the plating process, such as an evaporating process and a sputtering process.

After the metallic films 155 are formed, a resist removing step is carried out in which the resist pattern films 124a are removed. Hence, the lead frame 159 shown in Fig. 65 is formed.

Then, the semiconductor devices 150 are produced by using the lead frame 159 thus formed. First, the lower resin layer 153 is formed on the surface on which the plated recess portions 155 are formed. As shown in Fig. 66, a portion of the lower resin layer 153 in the recess portion 155 forms the resin projection 154.

Thereafter, as shown in Fig. 67, the through hole 157 is formed in the resin projection 154 of the lower resin layer 153. Hence, the metallic film 155 is exposed through the through hole 157.

Then, an electrically conductive metallic film 160 is formed to a given thickness on the entire surface of the lower resin layer 153, as shown in Fig. 68. The aforementioned connection electrodes 156 are derived from the metallic film 160. The metallic film 160 is formed by non-electrolytic plating, evaporating or sputtering. During the process of forming the metallic film 160, the metallic film 160 is filled in the through hole 157, so that the lower extending portion 162 is formed, as shown in Fig. 69. Hence, the metallic film 160 and the metallic film 155 are electrically connected together.

Subsequently, an etching resist film is coated on the metallic film 160 and exposing and developing steps are carried out. Then, as shown in Fig. 69, a resist pattern 161 is formed in the position in which the connection electrode 156 should be formed. Then, the metallic film 160 is etched so that the resist pattern 161 functions as a mask. Hence, the metallic film 160 is removed except for the

portions in which the connection electrodes 156 should be formed.

As shown in Fig. 70, the connection electrode 156 is formed which has a structure in which the lower extending portion 162 is connected to the metallic film 155, and the upper bonding portion 163 to which the wire 118 is to be bonded extends over the lower resin layer 153.

The remaining production steps following the step of forming the connection electrodes 156 are the same as corresponding ones which have been described with reference to Figs. 46 through 54B, and a description thereof will be omitted.

[Twelfth Embodiment]

A description will now be given of a semiconductor device according to a twelfth embodiment of the present invention.

Fig. 71 shows a semiconductor device 170 according to the twelfth embodiment of the present invention. In Fig. 71, parts that are the same as those of the semiconductor device 150 are given the same reference numbers.

The semiconductor device 170 has the resin package 151 of the two-layer structure including the upper resin layer 152 and the lower resin layer 153, and has metallic projections 171 integrally formed in connection electrodes 172. The metallic projections 171 are substituted for the resin projections 154. The single-layer metallic film 155 made of, for example, palladium (Pd) is provided to each of the metallic projections 171.

The connection electrodes 172 are provided to the lower resin layer 153. The metallic projections 171 are electrically connected to the corresponding metallic films 155 through windows (through holes) 173 formed in the lower resin layer

153. The bonding wires 118 are bonded to bonding portions 174 which are upper portions of the connection electrodes 172 and extend on the upper surface of the lower resin layer 153.

The semiconductor device 170 has the two-layer-structure resin package 151 as in the case of the semiconductor device 150, so that the characteristics of the semiconductor device 170 can be improved. Further, it is possible to decrease the impedance between the metallic projection 171 and the metallic film 155 because the metallic film 155 is directly connected to the metallic projection 171. Hence, the electrical characteristics of the semiconductor device 170 can further be improved. It should be noted that the resin package 151 is not limited to the two-layer structure and may have a structure consisting of three layers or more.

A description will now be given, with reference to Figs. 72 through 81, of a method of producing the semiconductor device 170. This method has particular features in the steps of forming the metallic films 155 and the connection electrodes 172, and has the other steps almost the same as those of the method of producing the semiconductor device 150. Hence, the following description is specifically directed to the steps of forming the metallic films 155 and the connection electrodes 172.

As shown in Fig. 72, the plate-shaped metallic member 121 made of copper (Cu) or the like is prepared. Next, etching resist films made of photosensitive resin are provided to two opposite surfaces of the metallic member 121. Then, the etching resist films are subjected to the exposing and developing processes, so that the resist patterns 124a having windows located in the positions in which the recess portions 158 should be formed can be formed, as shown in Fig. 73.

The metallic member 121 on which the resist patterns 124a are formed is etched (etching step). In this etching step, the metallic member 121 is half-etched from only the upper surface thereof. Hence, the recess portions 158 are formed in the metallic member 121, as shown in Fig. 74, which is an enlarged cross-sectional view of a part C shown in Fig. 73.

After the etching step is completed, a metallic film forming step is executed so that the metallic film 155 is formed in the recess portion 158 by plating, as shown in Fig. 75. Besides the plating process, an evaporating or sputtering process can be employed. Then, the resist patterns 124a are removed by the resist removing step, so that a lead frame 159 shown in Fig. 76 can be formed.

Then, the semiconductor devices 170 are derived from the lead frame 159. As shown in Fig. 77, the lower resin layer 153 is provided to the surface of the metallic member 121 on which the recess portions 158 are formed. Thereafter, as shown in Fig. 78, the portion of the lower resin layer 153 corresponding to the recess portion 158 is removed, so that a window or through hole 173 is formed therein. The metallic member 121 is exposed through the window 173.

Thereafter, the electrically conductive metallic film 160 is formed to a given thickness on the entire surface of the lower resin layer 153. The metallic film 160 can be formed by non-electrolytic plating, evaporating or sputtering. During the process of forming the metallic film 160, the metallic film 160 is filled in the through hole 158, so that the metallic projection 171 is formed, as shown in Fig. 79. Hence, the metallic film 160 and the metallic film 155 are electrically connected together.

The area of the window 173 is greater than the diameter of the through hole 157, so that a

greater contact area between the metallic projection 171 and the metallic film 155 can be obtained. Hence, the metallic projection 171 and the metallic film 155 can be electrically connected together with a lower impedance.

After forming the metallic film 160, an etching resist film is deposited thereon, and the exposing and developing processes are carried out. Hence, the resist pattern 161 located in the position in which the connection electrode 172 should be formed is formed. Then, the metallic film 160 is etched in such a way that the resist pattern 161 serves as a mask. Hence, the metallic film 160 is removed except for the portion covered by the mask.

Hence, as shown in Fig. 81, the connection electrode 172 is formed, the connection electrode 172 having a structure in which the metallic projection 171 is connected to the metallic film 155, and the bonding portion 174 to which the wire 118 is to be bonded extends over the lower resin layer 153.

The remaining production steps following the step of forming the connection electrodes 172 are the same as corresponding ones which have been described with reference to Figs. 46 through 54B, and a description thereof will be omitted.

[Thirteenth Embodiment]

A description will now be given, with reference to Fig. 82, of a semiconductor device 180 according to a thirteenth embodiment of the present invention. In Fig. 82, parts that are the same as those of the semiconductor device 150 are given the same reference numbers.

The semiconductor device 180 has a resin package 181 made up of an upper resin layer 182 and a lower resin layer 183, in which the lower resin layer 183 is formed by an insulation resin tape. Windows

184 are formed in given positions in the resin tape 183, and external electrode films 185 are formed to the lower surface (mounting surface) of the resin tape 183 so that the electrode films 185 cover the windows 184. The bonding wires 118 are bonded to the electrode films 185 through the windows 184.

The semiconductor device 180 has improved characteristics resulting from the two-layer package structure, and a cost reduction due to the resin tape 183 used instead of the lead frame 120 or 159.

[Fourteenth Embodiment]

A description will now be given of a semiconductor device according to a fourteenth embodiment of the present invention. Fig. 83 is a cross-sectional view of a semiconductor device 210 according to the fourteenth embodiment of the present invention. Fig. 84A is a plan view of the semiconductor device 210, Fig. 84B is a front view thereof, and Fig. 84C is a bottom view thereof.

The semiconductor device 210 has a simple structure including a chip 211, a resin package 212 and metallic films 213. A plurality of electrode pads 214 are formed on the upper surface of the chip 211, which is mounted on a chip fixing resin 215. The chip 211 may be a semiconductor chip, a SAW chip, a multichip module or the like.

The resin package 212 is formed by molding (or potting) an epoxy resin, and has resin projections 217 integrally formed with the other portion of the resin package 212. The resin projections 217 are located in given positions. Each of the resin projections 217 projects downwards from a bottom surface (mount-side surface) 216 of the resin package 212, and also projects laterally from a side surface 212a thereof. The resin projections 217 are arranged at a pitch approximately equal to, for example, 0.8

mm.

The metallic films 213 are provided so as to cover the respective resin projections 217. Bonding wires 218 are provided between the metallic films 213 and the electrode pads 214, and are electrically connected together. The metallic films 213 can be configured as shown in Figs. 35 through 38. The metallic films 213 may be configured as will be described later.

The semiconductor device 210 thus formed does not need any inner and outer leads used in the SSOP. Hence, there is no need to provide an area for leading the inner leads and a space in which the outer leads extend. Hence, a down-sized semiconductor device can be provided. Further, the semiconductor device 210 does not need any solder balls used in the BGA type, and is thus less expensive. Furthermore, the resin projections 217 and the metallic films 213 cooperate with each other as if they function as solder bumps of the BGA-type devices, so that a high mounting density can be obtained. Furthermore, the semiconductor device 210 is not affected by a curvature or deformation of the resin package 212.

The semiconductor device 210 has another advantage, which will now be described with reference to Fig. 85. Referring to Fig. 85, the semiconductor device 210 is mounted on a circuit board 250, on which connection electrodes 251 are provided in positions corresponding to those of the metallic films 213. The metallic films 213 are soldered to the connection electrodes 251. A reference number 219 indicates a solder portion. The solder portions 219 laterally extend along the metallic films 213 and laterally project from the resin package 212. Hence, the solder portions 219 can be visually checked, as shown in Fig. 85. This advantage facilitates the test of determining whether the semiconductor device 210 is

duly mounted on and soldered to the circuit board 250.

Each of the metallic films 213 can have one of the multilayer structures shown in Figs. 86, 87 and 88 which satisfy the aforementioned film requirement.

Fig. 86 shows a metallic film 213E having a five-layer structure consisting of an outer layer 213E-1, a first intermediate layer 213E-2, a second intermediate layer 213E-3, a third intermediate layer 213E-4, and an inner layer 213E-5. These layers can be made of the following combinations.

213E-1	213E-2	213E-3	213E-4	213E-5
Au	Pd	Ni	Pd	Au
solder	Ni	Au	Pd	Au
Pd	Ni	Au	Pd	Au
Pd	Ni	Cu	Ni	Pd
Au	Ni	Cu	Ni	Au
Au	Pd	Ni	Au	Pd

Fig. 87 shows a metallic film 213F having a six-layer structure consisting of an outer layer 213F-1, a first intermediate layer 213F-2, a second intermediate layer 213F-3, a third intermediate layer 213F-4, a fourth intermediately layer 213F-5, and an inner layer 213F-6. These layers can be made of the following combinations.

213F-1	213F-2	213F-3	213F-4	213F-5	213F-6
Au	Pd	Ni	Au	Pd	Au
Au	Pd	Ni	Cu	Ni	Pd
Pd	Ni	Cu	Ni	Pd	Au

Fig. 88 shows a metallic film 213G having a seven-layer structure consisting of an outer layer 213G-1, a first intermediate layer 213G-2, a second intermediate layer 213G-3, a third intermediate layer 213G-4, a fourth intermediate layer 213G-5, a fifth

intermediately layer 213G-6, and an inner layer 213G-7. These layers can be made of the following combinations.

213G-1	213G-2	213G-3	213G-4	213G-5	213G-6	213-7
Au	Pd	Ni	Cu	Ni	Pd	Au

In Figs. 86, 87 and 88, the aforementioned bonding balls 101 are depicted. The bonding balls 101 can be employed or can be omitted as shown in Fig. 83.

The semiconductor device 210 can be produced in the same manner as has been described with reference to Fig. 39 through 59.

Instead of the bonding balls 101, it is also possible to use stud balls or stud bumps as will be described below.

Fig. 89A shows a state observed when the chip mounting step, which has been described with reference to Fig. 46, is completed. A lead frame 220, produced in the aforementioned manner, includes recess portions 222, in which metallic films 213C having a three-layer structure shown in Fig. 37 are provided. The chip 211 having the electrode pads 214 is mounted on the chip fixing resin 215.

Fig. 89B shows a state in which stud bumps 245 are provided on the inner walls of the metallic films 213C. After forming the stud bumps 245, a capillary 246 is moved so as to be positioned just above the target electrode pad 214, as shown in Fig. 89C. In this state, the bonding wire 218 is bonded to the electrode pad 214 (first bonding). Then, the capillary 246 is moved so as to be positioned just above the target stud bump 245. By this movement, the bonding wire 218 is extended up to the position just above the stud bump 245.

Then, as shown in Fig. 89D, the capillary 246 is pressed by the stud bump 245, so that the

bonding wire 218 is bonded to the stud bump 245 (second bonding). The above process is repeatedly carried out in order to electrically connect the electrode pads 214 and the stud bumps 245 (the metallic films 213C) by the bonding wires 218, as shown in Fig. 89E.

The use of the stud bumps 245 improves the reliability of bonding as in the case of the use of the bonding balls 101. That is, the bonding wires 218 can be certainly bonded to the stud bumps 245, so that the electrical connections between the bonding wires 218 and the metallic films 213C can be highly reliable.

The stud bumps 245 can be formed as shown in Figs. 90A through 90I. In the following description, a gold wire is used as the bonding wire 218. For the sake of simplicity, Figs. 90A through 90I show the metallic film 213C and its vicinity.

First, as shown in Fig. 90A, the capillary 245 is moved and positioned above the metallic film 213C. Next, a spark is generated by using a spark rod (not show) provided in the wire bonding apparatus, so that a ball (having a diameter of, for example, 90 μm) is formed on the end of the wire 218.

Then, as shown in Fig. 90B, the capillary 245 is lowered so that the ball 247 is pressed. In this state, the ball 247 is bonded to the metallic film 213C by, for example, ultrasonic welding. The ball 247 is pressed and much deformed by the capillary 245, so that the ball 247 has a diameter of 10 - 120 μm and a height of 30 - 40 μm.

Subsequent to the above bonding step, as shown in Fig. 90C, the capillary 246 is raised by about 300 μm from the ball 247. Then, as shown in Fig. 90D, the capillary 246 is moved laterally by approximately 40 - 50 μm. Hence, the capillary 246 is positioned in an offset position laterally deviating

from the center of the ball 247.

Thereafter, as shown in Fig. 90E, the capillary 246 is lowered while the offset position is maintained, and crushes the ball 247. Then, in the state in which the wire 218 is clamped (no feeding of the wire 218 is carried out), as shown in Fig. 90F, the capillary 246 is raised. Hence, the wire 218 is cut and the stud bump 245 is formed.

In the above-mentioned manner of forming the stud bump 245, the capillary 245 crushes the ball 247, so that a tight contact between the stud bump 245 and the metallic film 213C can be made. Further, the ball 247 is made to have a wider area. Hence, as shown in Figs. 90G through 90I, the wider area of the ball 247 makes it possible to certainly perform the bonding process. The wire 218 and the stud bump 245 are of an identical substance (gold), and an excellent bondability can be obtained. Hence, the reliability of the joint between the wire 218 and the stud bump 245 can be highly improved.

As has been described with reference to Fig. 90F, the wire 218 is cut by the capillary 246 as it ascends after crushing the ball 247. At this time, the capillary 246 is in the offset position. Hence, the bonding is not affected due to the presence of a projection 248 (the remaining wire) extending upwards from the ball 247.

The wire 218 is not limited to gold, and can be formed of a coated gold wire with a gold core wire coated by an insulating member. The use of such a coated wire prevents shortcircuiting between the wire 218 and another portion. Hence, it is preferable to use the coated bonding wire if it is required to arrange the wires 218 at a high density.

As has been described previously, the semiconductor device 210 can be produced in the same manner as the semiconductor device 110. However, a

die used in the molding step has a shape slightly different of that of the die used in the method of producing the semiconductor device 210. This is because each of the resin projections 217 laterally extends from the package 212 as shown in Fig. 85.

Fig. 91 shows an upper die 256 and a lower die 257, which are used to form the resin package 212 by molding. The upper die 256 has a cavity 258, which has corner portions 258a. The corner portions 258 are located above the recess portions 222, so that the recess portions 222 are partially covered by the upper die 256. Hence, the resin projections 217 respectively having laterally extending portions which should be located at D in Fig. 91 can be formed.

As shown in Fig. 92, the upper die 256 has gates 232, and resin is supplied to pass through the gates 232, as indicated by the arrows. Hence, the resin package 212 is formed, as shown in Fig. 93, which corresponds to Fig. 50. It will be noted that a plurality of resin packages 212 are formed on the lead frame 220. A reference number 223 indicates tool engagement portions, which correspond to the tool engagement portions shown in Fig. 50.

An alternative separating step shown in Fig. 94 can be employed instead of the separating step shown in Fig. 53. An etching apparatus 260 shown in Fig. 94 includes a feed reel 261, an etching chamber 262, and a take-up reel 263. A plurality of lead frames 220 to which the resin packages 212 are provided are attached to a tape member 233, which is wound on the feed reel 261. Nozzles 264 for injecting etchant are provided in the etching chamber 262. The tape member 233 is fed from the feed reel 261 and is supplied to the etching chamber 262, in which the lead frame 262 facing the nozzles 264 is etched. By the etching process, the lead frame 220 is dissolved except for the metallic films 231C. Hence, the resin

packages 212 are separated from the lead frame 220.

The tape member 233 is formed of a material not affected by the etchant, so that the resin packages 212 are supported by the tape member 233 after the lead frame 220 is dissolved. The tape member 233 by which the packages 212 are supported goes out of the etching chamber 262, and is wound by the take-up reel 263. By using the above etching apparatus, it is possible to automatically separate the packages 212 from the lead frame 220.

The etching apparatus shown in Fig. 94 can be used to produce the semiconductor devices according to the other embodiments of the present invention.

It is possible to employ a separating step shown in Fig. 95 instead of the separating step shown in Fig. 53 or 59. The separating step shown in Fig. 95 employs the step of etching the lead frame 220 in such a way that the resin packages 212 are supported by a fixing tool 294. As shown in Fig. 95, the fixing tool 294 is made up of a plate-shaped base 295, and fixing pins 296 which stand upright. The lead frame 220 and the runner frames 234 have through holes 297 and 298 as shown in Fig. 96. More particularly, the through holes 297 are formed in the lead frame 220, and the through holes 298 are formed in the runner frames 234. As shown in Fig. 96, the through holes 297 and 298 are connected so that single holes can be respectively formed. The fixing pins 296 provided to the fixing tool 294 can be inserted into the through holes 297 and 298.

Fig. 97 shows one through hole 298 formed in the runner frame 234. Figs. 98A and 98B also show through holes 298 formed in the runner frames 234. A ring portion 299 is formed in the runner frame 234, and the through hole 298 is formed in the ring portion 299. Hence, the runner frames 234 having the through holes 298 in the ring portions 299 can have a given

mechanical strength. Hence, there is no possibility that the runner frames 234 may be broken in the through holes 298 and the resin packages 212 may be separated during the separating step.

Turning to Fig. 95 again, the fixing pins 296 are inserted into the through holes 297 and 298 so that the resin packages 212 face the base 295. Hence, the relative movement of the lead frame 220 and the fixing tool 294 is prevented. In this state, the resin packages 212, the runner frames 234 and the lead frame 220 are inserted, along with the fixing tool 294, into the etching chamber 262 shown in Fig. 94. The etchant is injected at a high pressure and the lead frame 220 is dissolved. During this process, the highly pressured etchant is applied to the resin packages 212 and the runner frames 234. However, the fixing tool 294 certainly supports the resin packages 212 and the runner frames 234, so that any displacement of these components cannot be caused due to the injection of the etchant. If these components are displaced, it will be necessary to place them back in the original positions. The fixing tool 294 is made of a material not affected by the etchant, and thus can be repeatedly used.

Figs. 99A, 99B and 99C show another separating step. As has been described previously, the runner frames 234 should be removed before shipping. The separating step shown in Figs. 99A, 99B and 99C has a particular step of removing the runner frames 234. A fixing tool 294A is used to maintain the resin packages 212 and the runner frames 234 in the stationary step. The fixing tool 294A has wall portions 2100, which stand upright on the base 295. The wall portions 2100 define a plurality of accommodating portions 2101 and 2102. As shown in Fig. 99A, the resin packages 212 face the resin package accommodating portions 2101, and the runner

frames 234 face the runner frame accommodating portions 2102.

In the state in which the resin packages 212 (runner frames 234) and the lead frame 220 are supported by the fixing tool 294A, the wall projections 2100 face the portions in which the resin packages 212 and the runner frames 234 are joined together. The above portions are thinner than the other portions, and do not have a mechanical strength as strong as the other thick portions. However, the relatively thin portions have a mechanical strength which is not broken by the injection of the highly pressured etchant.

Grooves 2103 are formed on the runner frames 234. As shown in Figs. 100A, 100B and 101, the groove 2103 extends in the center of the runner frame 234. The portions having the grooves 2103 are mechanically weaker than the other portions, but have a mechanical strength which prevents the runner frames 234 from being broken.

In the above separating step, the fixing tool 294A is positioned as shown in Fig. 99A. Since the resin packages 212 have a height different from that of the runner frames 234, the arrangement of the resin packages 212 and the runner frames 234 form step portions. The wall portions 2100 engage the recess portions of the step portions, so that the resin packages 212 can be prevented from deviating from the original positions.

As shown in Fig. 99A, a mesh member 2104 is provided on the surface of the lead frame 220 opposite to the surface thereof on which the runner frames 234 are formed. The mesh member 2104 allows the etchant to pass therethrough. Hence, the mesh member 2104 does not affect the step of etching the lead frame 220. Further, the mesh member 2104 is urged so as to press the lead frame 220 against the fixing tool 294A.

Hence, the resin packages 212, the runner frames 234 and the lead frame 220 can be certainly supported by the fixing tool 294A. Hence, it is possible to prevent occurrence of any positional error of the lead frame 220 in the etching process.

Fig. 99B shows that the lead frame 220 and the mesh member 2104 have been removed by the etching process. In Fig. 99B, the resin packages 212 and the runner frames 234 are joined together. Further, the resin packages 212 face the accommodating portions 2101, and the runner frames 234 face the accommodating portion 2102.

Then the resin packages 212 and the runner frames 234 are pressed so that the wall portions 2100 come into contact with the joint portions between the resin packages 212 and the runner frames 234. The joint portions are thinner than the other portions, and therefore are easily broken as shown in Fig. 99C without any excessive stress to the resin packages 212.

It should be noted that the resin packages 212 (semiconductor devices 210) can be accommodated in the accommodating portions 2101, and the broken runner frames 234 can be accommodated in the accommodating portions 2102. In this manner, the semiconductor devices 210 and the runner frames 234 can be automatically and separately accommodated, and thus the production process can be simplified.

Figs. 102A through 102E show yet another separating step. Fig. 102A shows that the resin packages 212 are supported by the lead frame 220. The runner frames 234 are not formed. As shown in Fig. 102B, a sheet member 2105 is provided so as to cover the resin packages 212 after the sealing step is carried out and before the lead frame 220 is removed. The sheet member 2105 is not supplied with any adhesive, while the aforementioned tape member 233 is

supplied with an adhesive.

Then, as shown in Fig. 102C, the sheet member 2105 is attached to the resin packages 212 by a vacuum absorbing process (sheet member absorbing step). Hence, the sheet member 2105 is deformed so as to match the shape of the resin packages 212 and is adhered thereto. Thus, the resin packages 212 are supported by the sheet member 2105. It should be noted that an adhesive is not used to support the resin packages 212 by the sheet member 2105.

Then, the packages 212 supported by the lead frame 220 and the sheet member 2105 are placed in the etching chamber 262, and the lead frame 220 is etched. Fig. 102D shows a state observed when the etching process is completed. The resin packages 2105 are supported by the sheet member 2105.

Finally, as shown in Fig. 102E, the resin packages 212 supported by the sheet member 2105 are accommodated in a package accommodating member container 2106, and an accommodating tool 2107 is driven so that the resin packages 212 are depressed one by one. Each of the resin packages 212 is separated from the sheet member 2105, and is then accommodated in the container 2106 (resin package accommodating step).

It should be noted that no adhesive is used to support the resin packages 212 by the resin sheet 2015, and thus the above package accommodating process can easily be carried out.

Instead of use of the container 2106, it is possible to perform a packing process as shown in Figs. 103A and 103B. After the assembly shown in Fig. 102D is obtained, a second sheet member 2108 is provided to the packages 212 so that the packages 212 are packed by the first and second sheet members 2105 and 2108 (packing step). The assembly shown in Figs. 103A and 103B can be handled by a packed product.

[Fifteenth Embodiment]

A description will now be given, with reference to Fig. 104, of a semiconductor device according to a fifteenth embodiment of the present invention. In Fig. 104, parts that are the same as those of the fourteenth embodiment of the present invention are given the same reference numbers.

A semiconductor device 210A shown in Fig. 104 has a feature in which resin projections 217A are provided on one side of the resin package 212. Such an arrangement of the resin projections 217A can be easily defined by appropriately selecting the positions of the recess portions 222 in the lead frame 220.

The semiconductor device 210A can be mounted on the circuit board 250 as follows. As shown in Fig. 104, through holes 252, to which electrical conductors are provided, are formed in the circuit board 250 so that the through holes 252 correspond to the resin projections 217A. The resin projections 217A are inserted into the through holes 252 so that the semiconductor device 210A stands upright. Then, the metallic films 213 respectively formed on the resin projections 217A are soldered to the conductors formed in the through holes 252. The above mounting manner increases the mounting density, since the semiconductor device 210A is vertically mounted. Further, it is easy to check, from the outside of the semiconductor device 210A, the states of soldering in the connections between the metallic films 213 and the conductors in the through holes 252.

[Sixteenth Embodiment]

Fig. 105 is a plan view of a semiconductor device 210B according to a sixteenth embodiment of the present invention, and Fig. 106 shows the

semiconductor device 210B mounted on the circuit board 250. In these figures, parts that are the same as those shown in the previously described figures are given the same reference numbers.

The semiconductor device 210B has a feature in which supporting members 253 are provided on one side of the resin package 212. The supporting member 253 supports the resin package 212 so that the semiconductor device 210 stands upright on the circuit board 250. The semiconductor device 210B has an alignment of resin projections 217B provided on one side of the resin package 212, as in the case of the semiconductor device 210A.

The semiconductor device 210B is mounded so that the resin projections 217B are positioned to the connection electrodes 251 formed on the circuit board 250, and are soldered thereto via the soldering portions 219. The above soldering can be carried out by a solder reflow process, so that the soldering process can be facilitated. The sixteenth embodiment of the present invention has the same advantages as those of the fifteenth embodiment thereof.

[Seventeenth Embodiment]

A description will now be given, with reference to Figs. 107 through 109, of a semiconductor device 210C according to a seventeenth embodiment of the present invention. In these figures, parts that are the same as those shown in the previously described figures are given the same reference numbers.

The semiconductor device 210C has a feature in which there are provided resin projections 291A and 291B having different lengths laterally. More particularly, the first resin projections 291A have a relatively short length, and the second resin projections 291B have a relatively long length.

Metallic films 290A are respectively provided to the first resin projections 291A, and metallic films 290B are respectively provided to the second resin projections 291B. The metallic films 290A are relatively short in the lateral direction, and the metallic films 290B are relatively long in the lateral direction. The second projections 291B and the second metallic films 290B extend below the chip 211.

The above arrangement of the resin projections 291A and 291B facilitates the routing of the bonding wires 218 toward the metallic films 290A and 290B. As shown in Fig. 107, the bonding wires 218 extend from the two sides of the chip 211 to the metallic films 290A and 290B. On the other hand, as shown in Fig. 104, the bonding wires 218 can be routed via only one side of the chip 211. Hence, it may be required that the electrode pads 214 formed on the chip 211 shown in Fig. 104 be aligned on one side of the chip 211. In the structure shown in Figs. 107 through 109, the electrode pads 214 can be arranged on four sides of the chip 211. Even in this case, the routing of the bonding wires 218 to the metallic films 290A and 290B provided on one side of the resin package 212 can be easily selected.

If the device 210C has the same number of electrode pads 214 as that of electrode pads 214 of the device 210A, the electrode pads 214 of the device 210C can be arranged at a pitch greater than that of the electrode pads of the device 210A. In other words, the device 210C can a larger number of electrode pads 214 than the device 210A at an identical pitch. Further, the electrode pads 214 and the metallic films 290A and 290B can be connected by relatively short bonding wires 218. Hence, short-circuiting between the wires 218 and an increase in the impedance of the wires 218 can be prevented.

[Eighteenth Embodiment]

Fig. 110 is a cross-sectional view of a semiconductor device 210D according to an eighteenth embodiment of the present invention, and Fig. 111 is a bottom view of the semiconductor device 210D. In these figures, parts that are the same as those shown in the previously described figures are given the same reference numbers.

The semiconductor device 210D has a feature in which the resin projections 291A are substantially flush with the side surface 212a of the resin package 212. The resin projections 291A are aligned on one side of the resin package 212 and have an identical lateral length. Hence, the metallic films 290A are aligned on one side of the resin package 212.

Even when the resin projections 291A are substantially flush with the side surface 212a, it is possible to visually check, from the side of the resin package 212, the states of soldering between the metallic films 290A and the circuit board.

The semiconductor device 210D can be mounted as shown in Fig. 112. A plurality of semiconductor devices 210D are arranged side by side so that the devices 210D stand upright. In this state, the semiconductor devices 210D are soldered to the circuit board 250. Supporting members 292 are respectively provided to the semiconductor devices 210D in order to support the semiconductor devices 210D. The supporting members 292 can be, for example, resin (adhesive), and are different from the supporting member 253 shown in Figs. 105 and 106. That is, the supporting members 292 are members separated from the resin packages 212, and are not integrally formed therewith. Hence, the positions of the supporting members 292 can be arbitrarily selected at an arbitrary time.

When the semiconductor devices 210D stand

upright and are arranged side by side, a space is defined between them. A spacer 293 can be provided between the above space before the semiconductor devices 210D are mounted on and fixed to the circuit board 250. The spacer 293 functions to more certainly make the semiconductor devices 210D stand upright on the circuit board 250 and to improve the reliability of mounting.

A mounting manner shown in Fig. 113 is characterized in that heat radiating members 293A are used instead of the spacer 293 shown in Fig. 112. The heat radiating members 293A radiate heat generated by the semiconductor devices 210D in addition to the function as spacers. It is preferable that the heat radiating members 293A are made of a material having a good thermal conductivity in order to realize good heat radiating performance. It is possible to efficiently and effectively radiate heat generated by the semiconductor devices 210D which are closely arranged side by side. Hence, the reliability of the operation of the semiconductor devices 210D can be improved.

Fig. 114 shows yet another mounting manner. The semiconductor devices 210D contact each other. This is achieved by making the semiconductor devices 210D stand on the circuit board 250 in an inclined state. The semiconductor devices 210D are inclined at an angle θ with respect to the circuit board 250. The semiconductor devices 210D are supported by the supporting members 292. The mounting manner shown in Fig. 114 needs no spacers and a smaller number of components necessary for mounting the semiconductor devices 210D. However, the heat radiation performance of the mounting method shown in Fig. 114 may not be as good as that of the mounting method shown in Fig. 113.

A plurality of semiconductor devices 210C can be arranged side by side so that they stand

upright on the circuit board 250, as shown in Fig. 115. In this case, the second resin projections 291B function spacers and heat radiating members. Hence, there is no need to use any spacers and heat radiating members.

[Nineteenth Embodiment]

A description will now be given, with reference to Figs. 116 and 117, of a semiconductor device according to a nineteenth embodiment of the present invention. Fig. 116 is a cross-sectional view of such a semiconductor device taken along a broken line shown in Fig. 117, which is a top view thereof in which the inner parts are seen through a resin package.

A semiconductor device 310 shown in Fig. 116 includes a chip 311, electrode pads 312, bonding wires 313, a resin package 314, and metallic films 315. The chip 311 may be a semiconductor chip, a SAW chip, a multichip module or the like. Ends of the bonding wires 313 are bonded to the electrode pads 312 on the chip 311, and the other ends thereof are bonded to the metallic films 315, which are exposed from the bottom surface of the resin package 314 formed by resin molding. The metallic films 315 substantially flush with the bottom surface of the resin package 315. Each of the metallic films 315 is, for example, 0.4 mm wide, 0.75 mm long, and 10 µm high, and are arranged at a pitch equal to, for example, 0.65 mm.

The above structure does not require the inner leads and outer leads necessary for the SSOP, so that there is no need to provide a leading area in which the inner leads are arranged as well as an area occupied by the outer leads. Further, the structure shown in Fig. 3 does not require a mount base necessary for providing solder balls in the BGA type. Hence, the semiconductor device according to the first

embodiment of the present invention requires a smaller mounting area and is less expensive.

The metallic films 315 are electrically connected to the chip 311 through the bonding wires 313. The metallic films 315 function as external connection terminals of the semiconductor device 310. When the semiconductor device 310 is mounted on a circuit board (not shown), the metallic films 315 are soldered to electrode portions provided on the circuit board.

The metallic films 315 can have a single-layer structure or a multilayer structure, as in the case of the aforementioned metallic films 113 and 213. It is required that the metallic films 315 satisfy the aforementioned film requirement.

Fig. 118 is an enlarged cross-sectional view of a metallic film 315A having a single-layer structure. The metallic film 315A can be made of, for example, silver (Ag) or palladium (Pd).

Fig. 119 is an enlarged cross-sectional view of a metallic film 315B having a two-layer structure consisting of an outer layer 315B-1 and an inner layer 315B-2. For example, the outer layer 315B-1 is a palladium layer having a thickness of 0.05 - 2 μm, and the inner layer 315B-2 is a gold layer having a thickness of 10 Å - 0.5 μm. The outer layer 315B-1 may be gold, and the inner layer 315B-2 may be palladium.

Fig. 120 is an enlarged cross-sectional view of a metallic film 315C having a three-layer structure consisting of an outer layer 315C-1, an intermediate layer 315C-2, and an inner layer 315C-3. By way of example, these layers can be configured as follows. The outer layer 315C-1 is a gold layer having a thickness of 10 Å - 0.5 μm, and the intermediate layer 315C-2 is a nickel layer having a thickness of 0.5 - 20 μm. The inner layer 315C-3 is a gold layer having

a thickness of 0.1 - 0.5 μm.

The following other combinations can be employed.

315C-1	315C-2	315C-3
Au	Ni	Au
Pd	Ni	Pd
Au	Pd	Au
solder	Ni	Au
solder	Ni	Pd

Fig. 121 is an enlarged cross-sectional view of a metallic film 315D having a four-layer structure consisting of an outer layer 315D-1, a first intermediate layer 315D-2, a second intermediate layer 315D-2, and an inner layer 315D-4. For example, the four-layer structure is as follows. The outer layer 315D-1 is a solder layer having a thickness of 5 - 20 μm, and the first intermediate layer 315D-2 is a nickel layer having a thickness of 1 - 20 μm. The second intermediate layer 315D-3 is a palladium layer having a thickness of 0.05 - 2 μm, and the inner layer 315D-4 is a gold layer having a thickness of 10 Å - 0.5 μm.

By way of another example, the outer layer 315D-1 is a palladium layer having a thickness of 0.05 - 2 μm, and the first intermediate layer 315D-2 is a nickel layer having a thickness of 1 - 20 μm. The second intermediate layer 315D-3 is a palladium layer having a thickness of 10 Å - 0.5 μm, and the inner layer 315D-4 is a gold layer having a thickness of 10 Å - 0.5 μm.

The following other combinations can be employed.

315D-1	315D-2	315D-3	315D-4
Au	Pd	Ni	Pd

Pd	Ni	Au	Pd
solder	Ni	Au	Pd

Alternatively, it is possible to form the metallic films 315 having a five-layer structure respectively made of substances described with reference to Fig. 86 or having a six-layer structure respectively made of substances described with reference to Fig. 87.

It is possible to employ the aforementioned bonding balls 101 to which the ends of the bonding wires 313 are bonded.

The above-mentioned semiconductor device 310 can be formed by using a lead frame 320 as shown in Fig. 125. In order to simultaneously produce a plurality of semiconductor devices 310, the lead frame 320 is configured as shown in aforementioned Fig. 42A, or a lead frame unit as shown in Fig. 43 having a plurality of lead frames as shown in Fig. 42 is used.

The lead frame 320 can be configured as follows. As shown in Fig. 122, a resist coating step is carried out so that etching resist films 324 are provided to two opposite surfaces of a metallic member 321 having tool engagement holes 323 (which correspond to the holes 123 shown in Fig. 42A).

Next, exposing and developing steps are carried out in order to obtain a structure having resist patterns 324a shown in Fig. 123. In the exposing step, a mask having windows corresponding to the positions of the metallic films 315 is provided on one of the etching resist films 324. In the developing step, the exposed portions of the etching resist film 324 are removed. The portions of the etching resist film 324 corresponding to the power supply portions 125 shown in Fig. 42A are also removed by the exposing and developing steps.

Thereafter, a metallic film forming step is carried out so that a structure shown in Fig. 124 is formed The above step is, for example, a plating process in which plating electrodes are provided to the power supply portions 125 shown in Fig. 42A, and the metallic member 321 is placed in a plating chamber. The structure shown in Fig. 124 is the three-layer structure 315C having the outer layer 315C-1, the intermediate layer 315C-2 and the inner layer 315C-3. In this case, the metallic member 321 is plated with gold to form the inner layer 351C-3. Next, the inner layer 351C-3 is plated with palladium to form the intermediate layer 351C-2. Then, the intermediate layer 351C-2 is plated with gold to form the outer layer 351C-1. The thickness of each of the above three layers can be regulated by controlling the plating time.

In the separating step to be carried out later, it is necessary to separate the metallic films 351C from the lead frame 320 together with the resin package 312. Hence, it is required that the metallic films 351C have a nature which enables the metallic films 351C to be smoothly separated from the metallic member 321. With the above in mind, a material which facilitates the separating process, such as an electrically conductive paste, is provided in the exposed portions of the metallic member 321 before the metallic films 351C are formed therein. Hence, the metallic films 351C are formed on the material.

It should be noted that the metallic films 351C can be formed by thin-film forming processes other than the plating process, such as an evaporating process and a sputtering process.

Then, the resist patterns 324a (the etching resist films 324) are removed by a resist removing step, so that the lead frame 320 shown in Fig. 125 can be formed.

The semiconductor device 310 can be produced by using the lead frame shown in Fig. 125.

As shown in Fig. 126, a chip mounting step is carried out in which a chip fixing resin 316 is provided in a given position on the lead frame 320, and the chip 311 is placed on the chip fixing resin 316. The chip fixing resin 316 functions as an insulation member and an adhesive. Hence, the chip 311 is mounted on the lead frame 320 due to the adhesiveness of the chip fixing resin 316.

Next, the lead frame 320 is loaded to the wire bonding apparatus, and the bonding wires 313 are provided as shown in Fig. 127. More particularly, the bonding wires 313 are bonded to the electrode pads 312 and the metallic films 315. The previously given description of the order of bonding the wires (the first and second bondings) holds true for bondings of the bonding wires 313. For example, if the ends of the bonding wires 313 are bonded to the metallic films 315C first, and the other ends thereof are bonded to the electrode pads 312 second, the height of the bonded wires 313 shown in Fig. 128 can be lower than that of the bonding wires 313 bonded in the reverse order shown in Fig. 127.

Then, the molding step is carried out in the same manner as that described with reference to Fig. 49. By the molding step, the resin package 314 is provided to each of the chips 311, as shown in Fig. 129. The lead frame 320 observed after the molding step is as shown in aforementioned Figs. 51A and 51B.

Thereafter, a tape arrangement step is carried out in the same manner as that already described with reference to Figs. 52A and 52B.

Then, a separating (etching) step which corresponds to the separating step shown in aforementioned Fig. 53 is carried out, as shown in Fig. 130 in which a reference number 333 indicates a

tape member which corresponds to the tape member 133 shown in aforementioned Fig. 53.

The semiconductor devices 310 observed after the lead frame 320 are supported by the tape member 333, as shown in aforementioned Figs. 54A and 54B.

An alternative separating step shown in Fig. 131 can be carried out in the same manner as shown in aforementioned Fig. 59.

In the above-mentioned production process, the semiconductor devices 310 can be produced.

[Twentieth Embodiment]

Figs. 132A and 132B show a semiconductor device 310B according to a twentieth embodiment of the present invention. In these figures, parts that are the same as those of the semiconductor device 310 are given the same reference numbers. The semiconductor device 310B differs from the semiconductor device 310 as follows. The metallic films 315 are formed on resin projections 318 which are portions of the resin package 314. An insulating film 317 is provided on the bottom surface of the resin package 314. Further, the metallic films 315 have lead portions 3151 extending toward the chip 311. The resin projections 318 can absorb a curvature of the resin package 314 when the semiconductor device 310B is mounted on a circuit board and can prevent occurrence of a solder bridge over adjacent metallic films. The leading portions 3151 extending toward the chip 311 enable a greater pitch at which the metallic films 315 are arranged.

This advantage is effective particularly to an area bump type in which the resin projections 318 are arranged on the entire bottom surface of the package 314. In this case, the area bumps can be arranged at a reduced pitch without bonding wires to recess portions arranged at a small pitch. The

insulating film 317 defines an area to be soldered when the semiconductor device 310B is mounted on a circuit board. Further, the insulating film 317 prevents a degradation of the semiconductor device 310B due to oxidation of the leading portions 3151. Furthermore, the insulating film 317 prevents occurrence of the solder bridge.

The semiconductor device 310B can be produced by almost the same process as that of producing the semiconductor device 310. The resin projections 318 can be defined by half-etching the metallic member 321 to which the resist patterns 324a are provided (Fig. 123). By the half-etching, recess portions like the recess portions 122 shown in Fig. 41 can be formed. The metallic films 315 can be provided to the above recess portions as shown in Fig. 44, so that the metallic films 315 can be formed on the resin projections 318. The wire bonding can be carried out, as shown in Fig. 47. The insulating film 317 can be formed by remaining the patterned resist film used to define the leading portions 3151.

[Twenty-first Embodiment]

Fig. 133 shows a semiconductor device 310C according to a twenty-first embodiment of the present invention. In Fig. 133, parts that are the same as those of the semiconductor device 310B shown in Figs. 132A and 132B are given the same reference numbers. A heat radiating member 340 is provided to the semiconductor device 310B. The heat radiating member 340 is made of a member having a good thermal conductivity. It is preferable that the insulating film 317 shown in Fig. 132A be omitted because the insulating film 317 may prevent heat radiating.

The heat radiating member 340 is adhered to the given portion of the lead frame, and then the chip 311 is fixed to the heat radiating member 340. The

use of the heat radiating member 340 makes it possible to mount a chip which consumes a large amount of power.

[Twenty-second Embodiment]

Fig. 134 shows a semiconductor device 310D according to a twenty-second embodiment of the present invention. In Fig. 134, parts that are the same as those of the semiconductor devices 310B and 310C are given the same reference numbers. The semiconductor device 310D employs bumps or bonding balls 341, which are replaced by the leading portions 3151 of the metallic films 315. The bumps 341 are provided in the projections and are connected to the metallic films 315. The structure shown in Fig. 134 will be effective to a case where the resin projections 318 are not arranged at a narrow pitch. The bumps 341 can more certainly connect the bonding wires 313 to the metallic films 315. The heat radiating member 340 can be used in the semiconductor device 310D in the same manner as shown in Fig. 133.

[Twenty-third Embodiment]

Fig. 135 shows a semiconductor device 310E according to a twenty-third embodiment of the present invention. In Fig. 135, parts that are the same as those shown in the previously described figures are given the same reference numbers. The semiconductor device 310E does not use bonding wires which connect the electrode pads 312 and the metallic films 315. Instead of such bonding wires, bumps 342 are used to electrically connect the electrode pads 312 and the metallic films 315. The use of the bumps 342 makes it possible to reduce the height of the semiconductor device 310E and to provide a thinner package. The bumps 342 can be provided by flip-chip bonding, which is faster than wire bonding. Hence, it is possible to

reduce the time necessary to connect the electrode pads 312 and the metallic films 315 together.

The semiconductor device 310E can be produced in almost the same manner as that of producing the semiconductor device 310 except for the following. When the chip 311 is mounted on the lead frame 320, the flip-chip bonding is carried out so that the electrode pads 312 are connected to the metallic films 315 via the bumps 342, which can be preformed to either the electrode pads 312 or the metallic films 315.

As shown in Fig. 136A showing a semiconductor device 310F, the bonding wires 313 of the semiconductor device 310B shown in Fig. 132 can be replaced by bumps 342. The flip-chip bonding is carried out for the leading portions 3151 of the metallic films 315. It is possible to increase the pitch at which the metallic films 315 provided on the resin projections 318 are arranged.

Fig. 136B shows a semiconductor device 310G, which is a variation of the structure shown in Fig. 136A. Referring to Fig. 136B, recess portions 343 are formed in the leading portions 3151 of the metallic films 315, and the bumps 342 are provided so as to engage the recess portions 343 by the flip-chip bonding. The use of the recess portions 343 facilitates the positioning of the bumps 342.

In the structures shown in Figs. 136A and 136B, the insulating films 317 can be omitted.

Fig. 137 shows a semiconductor device 310H, in which the bumps 342 are provided in the resin projections 318. The height of the resin projections 318 is less than that of the bumps 342 in order to directly connect the electrode pads 312 to the bumps 342. The bumps 342 are engaged with the recess portions formed in the lead frame, so that the positioning of the bumps 342 can be facilitated.

Fig. 138 shows a semiconductor device 310I in which the back surface of the chip 311 is exposed from the resin package 314. It is easily possible to radiate heat generated in the chip 311 to the outside of the semiconductor device 310I. The structure shown in Fig. 138 can be applied to the semiconductor devices shown in Figs.135, 136A and 136B.

Fig. 139A shows a semiconductor device 310J, in which a heat radiating member 345 is attached to the back surface of the chip 311 by means of an adhesive 344. The heat radiating performance can be facilitated by the heat radiating member 345.

Fig. 139B shows a semiconductor device 310K having the heat radiating member 345, which has a plurality of fins 346. The heat radiating performance can further be facilitated.

Fig. 140 shows a semiconductor device 310L, which has an insulating member 347 which is flush with the bottom surface of the resin package 314. The insulating member 347 can be formed of a tape, an adhesive or the like. The insulating member 347 is provided taking into account a possibility that it may be difficult for the mold resin to enter the gap between the chip 311 and the lead frame 320 in the resin molding step because the above gap is very small. In this case, the sealing may be defective. The insulating member 347 provided beforehand to the element forming surface of the chip 311 prevents occurrence of defective sealing even if the gap is completely full of the mold resin. The insulating member 347 can be provided to either the chip 311 or the lead frame 320 before the flip-chip bonding is carried out.

Fig. 141A shows a semiconductor device 310M in which the bumps 342 and the metallic films 315 are electrically and mechanically joined together by anisotropically electrically conductive resins 348.

The bumps 342 are provided to the electrode pads on the chip 311. As shown in Fig. 141C, the bumps 342 can be provided on the metallic films 315. Alternatively, it is possible to provide bumps 342a on the electrode pads, and bumps 342b on the metallic films 315. The resin 348 is provided to cover the bumps 342, 342a and 342b.

When a pressure is applied to the resins 342, fine conductors (conductive particles) contained in the resins 348 are made to be jointed together between the bumps 342 and the metallic films 315, so that the electrical connections can be made.

As shown in Fig. 141B, the bumps 342 are provided on the sides of the metallic frames 315 of the lead frame 320. As shown in Fig. 141C, bumps 342a are provided to the electrode pads on the chip 311, and bumps 342b are provided on the metallic films 315.

The use of the anisotropically electrically conductive resins 342 prevents a short-circuit between adjacent bumps, which may occur when the semiconductor device is mounted on a circuit board.

The present invention is not limited to the specifically disclosed embodiments, and variations and modifications may be made without departing from the scope of the present invention.

WHAT IS CLAIMED IS:

1. A device comprising:

a chip;

a resin package sealing said chip, said resin package having resin projections located on a mount-side surface of the resin package;

metallic films respectively provided to the resin projections; and

connecting parts electrically connecting electrode pads of said chip and the metallic films.

2. The device as claimed in claim 1, wherein each of said metallic films is a single layer made of a metallic substance.

3. The device as claimed in claim 1, wherein each of said metallic films comprises a plurality of metallic layers which are stacked.

4. The device as claimed in claim 1, wherein said connecting parts respectively comprise bonding wires, which are bonded to the electrode pads and said metallic films.

5. The device as claimed in claim 1, wherein:

said connecting parts respectively comprise bonding wires, and bonding balls respectively provided to the metallic films; and

said bonding wires are bonded to said electrode pads and said bonding balls.

6. The device as claimed in claim 1, wherein said resin package is a molded package so that the resin projections are integrally formed.

7. The device as claimed in claim 1, wherein said resin package includes a first resin portion on which the chip is provided, and a second resin portion which covers the chip.

8. The device as claimed in claim 7, wherein:

said connecting parts respectively comprise bonding wires, and connection electrodes which are provided on said first resin portions and extend, into the resin projections, to the metallic films; and

said bonding wires are bonded to the electrode pads and the connection electrodes.

9. The device as claimed in claim 8, wherein said resin projections respectively have through holes through which the connection electrodes extend to the metallic films.

10. A device comprising:

a chip;

a resin package sealing said chip and having a first resin portion and a second resin portion, said chip being provided on said first resin portion and covered by said second resin portion;

connecting parts having bonding wires and connection electrodes, said connection electrodes being provided on the first resin portion and projecting therefrom; and

metallic films respectively provided to the connection electrodes of said connecting parts.

11. A device comprising:

a chip;

a resin package sealing said chip and having a first resin portion and a second resin portion, said chip being provided on said first resin portion and covered by said second resin portion, the first resin portions having through holes;

electrode parts provided to said first resin portion so as to respectively cover the through holes; and

connecting parts connecting electrode pads of said chip and said electrode parts.

12. The device as claimed in claim 11, wherein said first resin portion comprises a resin tape.

13. The device as claimed in claim 11, wherein said connecting parts respectively comprise bonding wires, which are bonded to the electrode pads and the electrode parts.

14. A device comprising:

a chip;

a resin package sealing said chip, said resin package having resin projections located on a mount-side surface of the resin package, said resin projections extending downwards from the mount-side surface and laterally extending from at least one side surface of the resin package;

metallic films respectively provided to the resin projections; and

connecting parts electrically connecting electrode pads of said chip and the metallic films.

15. The device as claimed in claim 14, wherein each of said metallic films is a single layer made of a metallic substance.

16. The device as claimed in claim 14, wherein each of said metallic films comprises a plurality of metallic layers which are stacked.

17. The device as claimed in claim 14, wherein said connecting parts respectively comprise bonding wires, which are bonded to the electrode pads and said metallic films.

18. The device as claimed in claim 14, wherein:

said connecting parts respectively comprise bonding wires, and bonding balls respectively provided to the metallic films; and

said bonding wires are bonded to said electrode pads and said bonding balls.

19. The device as claimed in claim 14, wherein said resin package is a molded package so that the resin projections are integrally formed.

20. The device as claimed in claim 14, wherein said resin projections laterally extend from a plurality of side surfaces of said resin package.

21. The device as claimed in claim 14, wherein said resin projections laterally extend from only one side surface of said resin package.

22. The device as claimed in claim 20, further comprising supporting members provided to said resin package, said supporting members supporting the device vertically mounted on a circuit board.

23. A device comprising:

a chip;

a resin package sealing said chip, said resin package having resin projections located on a mount-side surface of the resin package, said resin projections extending downwards from the mount-side surface and being substantially flush with a side surface of the resin package;

metallic films respectively provided to the resin projections; and

connecting parts electrically connecting electrode pads of said chip and the metallic films.

24. The device as claimed in claim 23, wherein:

said resin projections comprise first projections and second projections being laterally longer than the first projections so that the second projections extend below the chip; and

said metallic films comprise first metallic films provided on the first projections, and second metallic films provided on the second projections.

25. The device as claimed in claim 23, further comprising a spacer to be provided to the mount-side surface of said resin package, wherein said spacer is in contact with another device when said device is supported on a circuit board so that said side surface of the resin package faces the circuit board.

26. The device as claimed in claim 25, wherein said spacer is a heat radiating member.

27. A method of producing devices respectively having chips sealed by resin packages, said method comprising:

(a) forming a lead frame having a base having recess portions respectively having metallic films;

(b) mounting chips on the lead frame;

(c) providing connecting parts which electrically connect electrode pads of said chips and the metallic films;

(d) molding resin so that molded resin packages respectively cover the chips and metallic films supported by the lead frame; and

(e) separating from the lead frame the molded resin packages together with the metallic films provided to resin projections which are counterparts of said recess portions.

28. The method as claimed in claim 27, wherein said step (e) comprises a step of etching the lead frame and thereby dissolving the lead frame.

29. The method as claimed in claim 27, wherein said step (e) comprises a step of mechanically separating the lead frame from the molded resin packages and the metallic films.

30. The method as claimed in claim 27, further comprising a step of providing a tape member to the molded resin packages before said step (e) is executed.

31. The method as claimed in claim 27, wherein said step (c) comprises a first step of providing bonding balls to the metallic films, and a second step of bonding bonding wires to electrode pads of the chip and said bonding balls, said bonding balls and said bonding wires corresponding to said

connecting parts.

32. The method as claimed in claim 27, wherein said step (d) molds the resin so that the molded resin packages are joined together.

33. The method as claimed in claim 27, wherein said step (d) molds the resin so that the molded resin packages are separated from each other.

34. A device comprising:

a chip;

a resin package sealing said chip, said resin package having a mount-side surface of the resin package;

metallic films respectively provided in the resin package so that the metallic films are flush with the mount-side surface and are exposed therefrom; and

connecting parts electrically connecting electrode pads of said chip and the metallic films.

35. The device as claimed in claim 34, wherein:

said connecting parts respectively comprise

bonding wires, and bonding balls respectively provided to the metallic films; and

said bonding wires are bonded to said electrode pads and said bonding balls.

36. The device as claimed in claim 34, wherein each of said metallic films is a single layer made of a metallic substance.

37. The device as claimed in claim 34, wherein each of said metallic films comprises a plurality of metallic layers which are stacked.

38. The device as claimed in claim 34, wherein said connecting parts respectively comprise bumps provided between the electrode pads of the chip and the metallic films.

39. A method of producing devices respectively having chips sealed by resin packages, said method comprising:

(a) forming a lead frame having a base on which metallic films are formed;

(b) mounting chips on the lead frame;

(c) providing connecting parts which

electrically connect electrode pads of said chips and the metallic films;

(d) molding resin so that molded resin packages respectively cover the chips and metallic films supported by the lead frame; and

(e) separating from the lead frame the molded resin packages together with the metallic films so that the chips are exposed from mount-side surfaces of the molded resin packages.

40. The method as claimed in claim 39, wherein said step (e) comprises a step of etching the lead frame and thereby dissolving the lead frame.

41. The method as claimed in claim 39, wherein said step (e) comprises a step of mechanically separating the lead frame from the molded resin packages and the metallic films.

42. The device as claimed in claim 1, wherein:

said metallic films respectively have lead portions, which are sealed by the resin package and extend toward the chip; and

said connecting parts include bonding wires which are bonded to said lead portions.

43. The device as claimed in claim 42, further comprising a heat radiating member sealed by the resin package, the chip being provided on said heat radiating member.

44. The device as claimed in claim 1, wherein:

said connecting members respectively comprise bumps provided between the electrode pads of the chip and the metallic films.

45. The device as claimed in claim 1, wherein:

said metallic films respectively have lead portions, which are sealed by the resin package and extend toward the chip; and

said connecting parts include bumps provided between the electrode pads of the chip and the lead portions of the metallic films.

46. The device as claimed in claim 1, wherein:

said metallic films respectively have lead portions, which are sealed by the resin package and extend toward the chip, said lead portions having recess portions; and

said connecting parts include bumps, which are positioned in said recess portions and are

provided between the electrode pads of the chip and the lead portions of the metallic films.

47. The device as claimed in claim 44, wherein a back surface of the chip opposite to a surface on which the electrode pads are provided is exposed from a surface of the resin package opposite to the mount-side surface thereof.

48. The device as claimed in claim 47, further comprising a heat radiating member attached to the back surface of the chip.

49. The device as claimed in claim 44, further comprising an insulating member provided to a surface of the chip on which the electrode pads are provided.

50. The device as claimed in claim 44, wherein said connecting parts comprise an electrically conductive resin containing conductive particles joined together under a given pressure.

ABSTRACT OF THE DISCLOSURE

A device includes a chip, and a resin package sealing the chip, the resin package having resin projections located on a mount-side surface of the resin package. Metallic films are respectively provided to the resin projections. Connecting parts electrically connect electrode pads of the chip and the metallic films.

FIG.1A

PRIOR ART

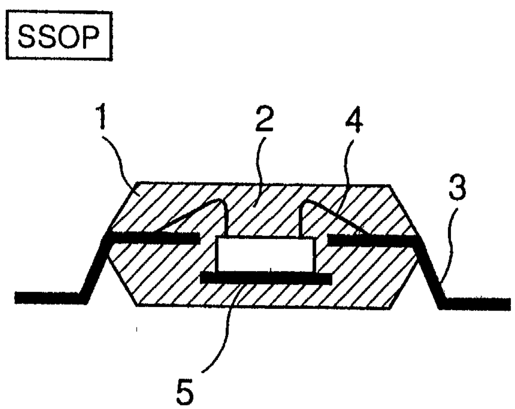


FIG.1B

PRIOR ART

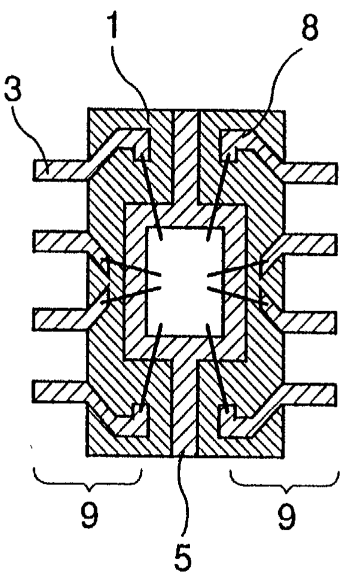


FIG.1C

PRIOR ART

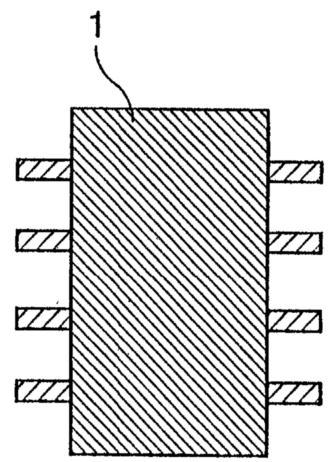


FIG.2

PRIOR ART

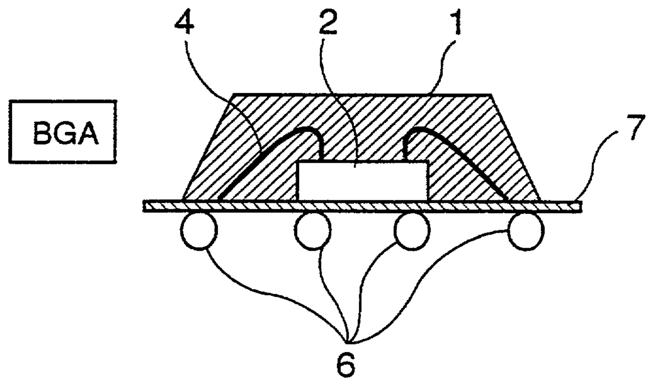


FIG.3

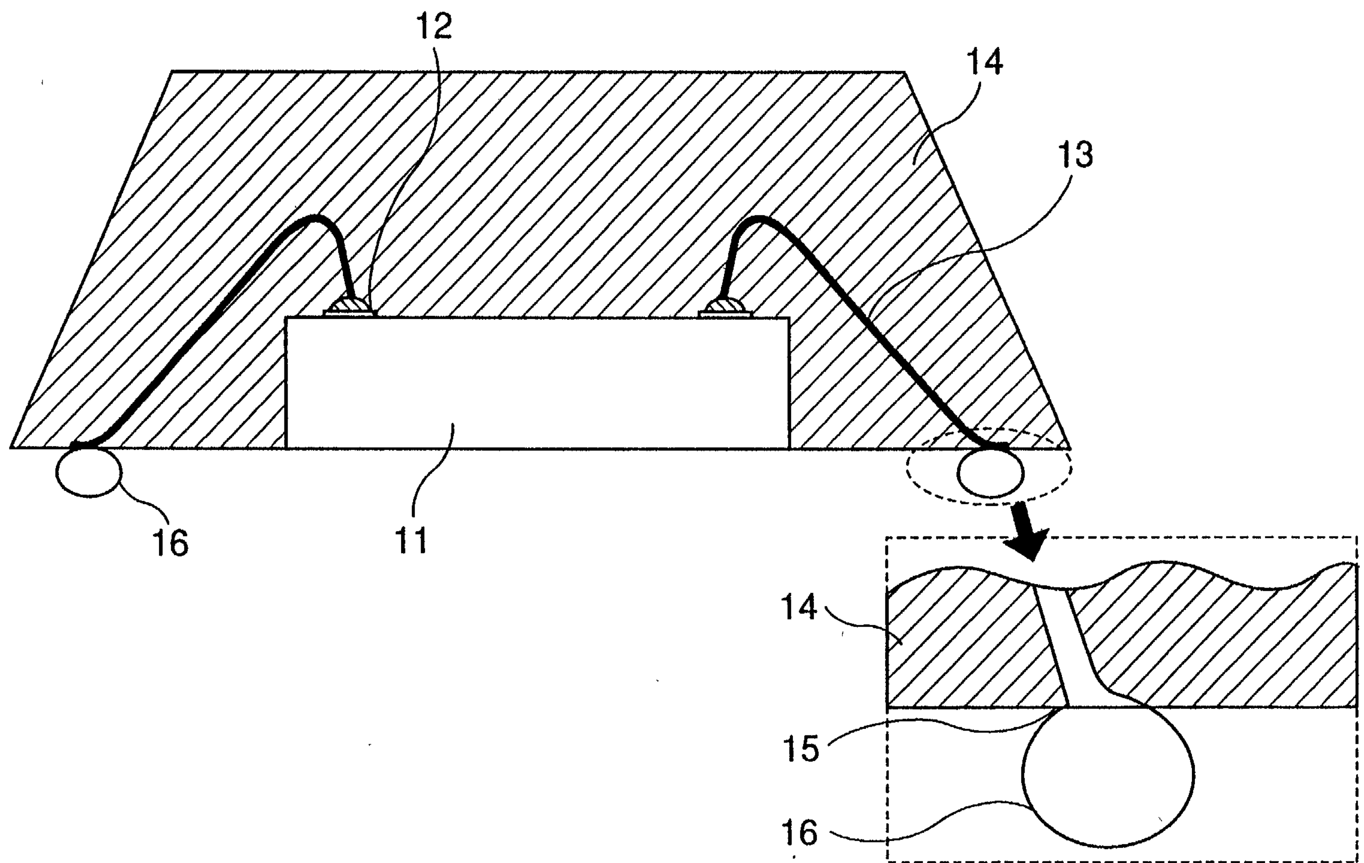


FIG.4

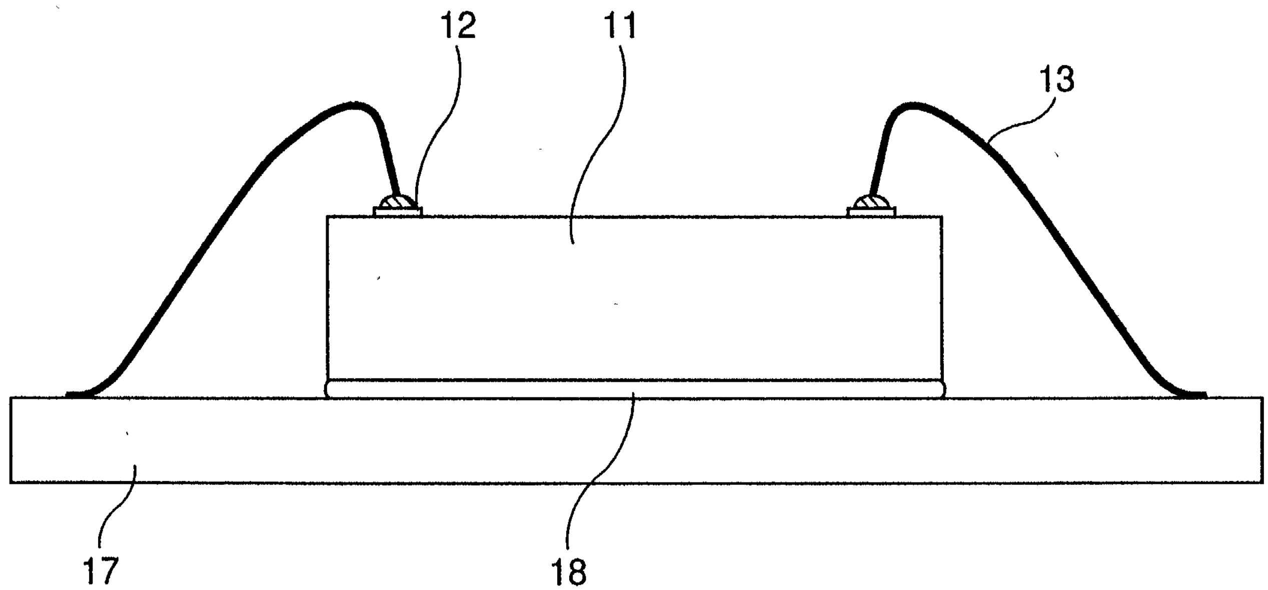


FIG.5

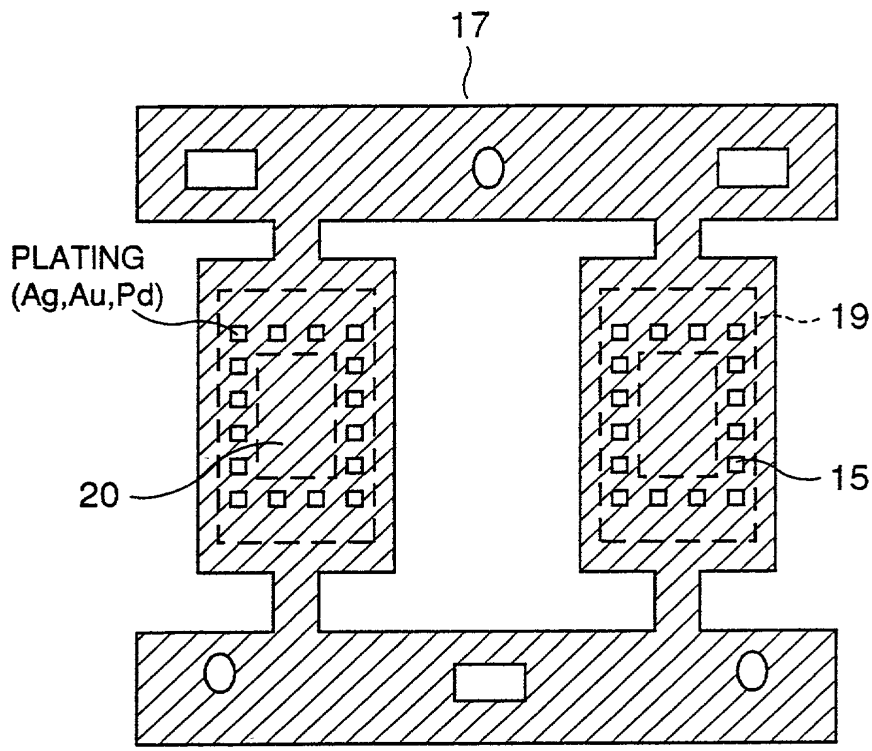


FIG.6

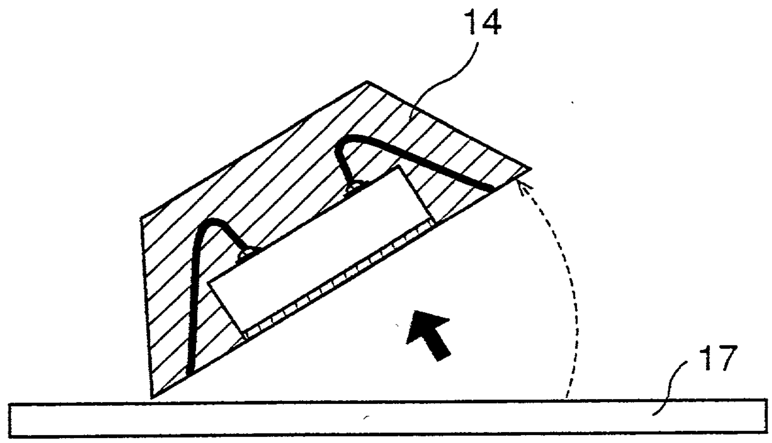


FIG.7

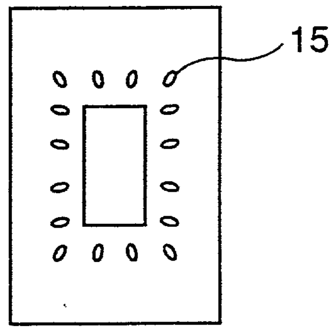


FIG.8

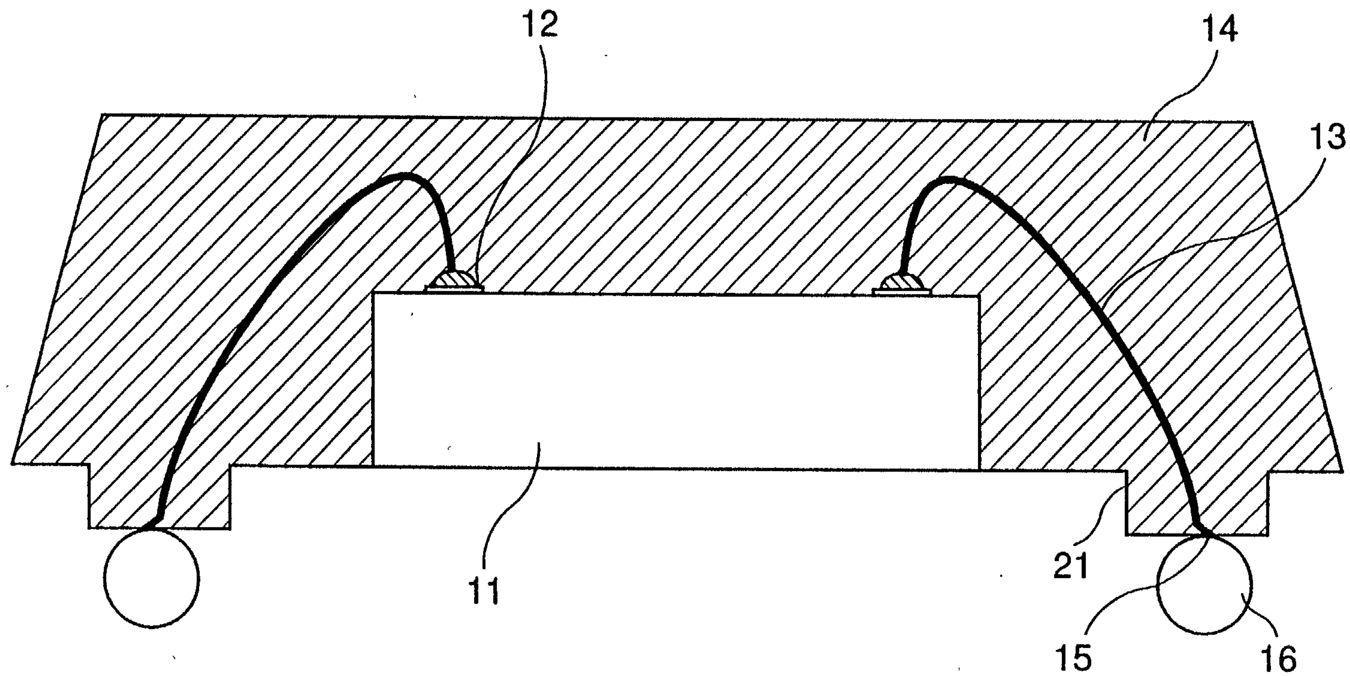


FIG.9

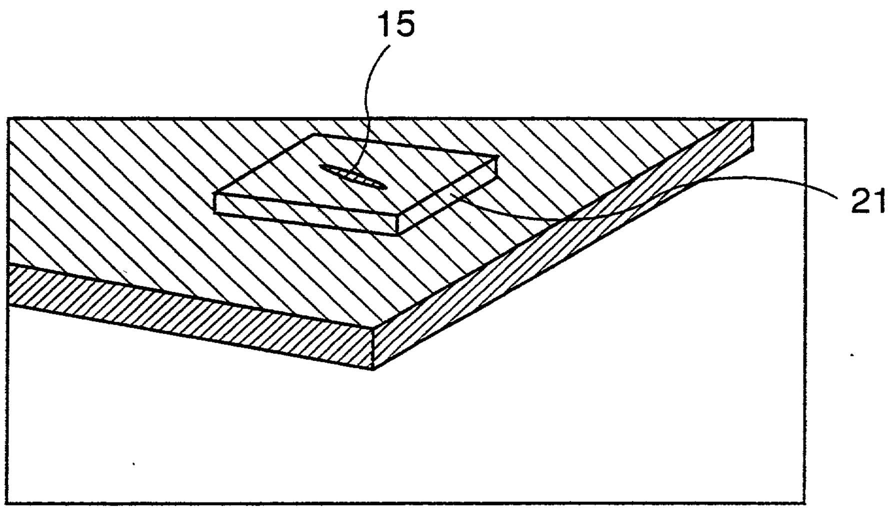


FIG.10

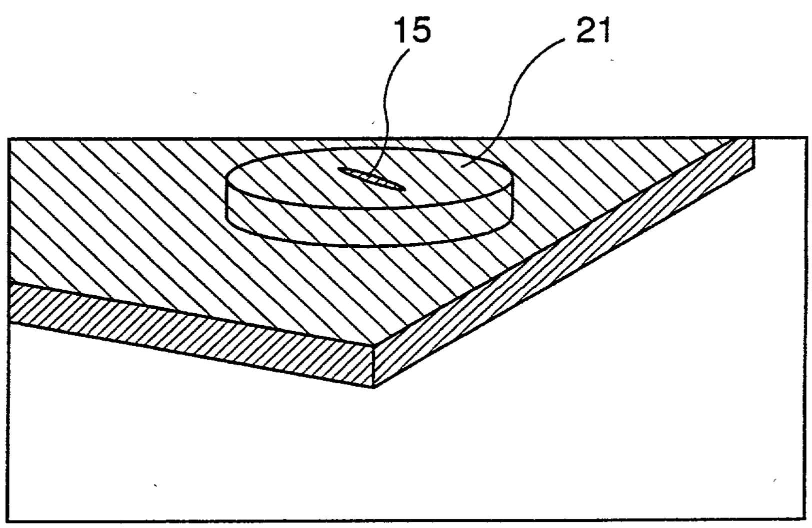


FIG.11

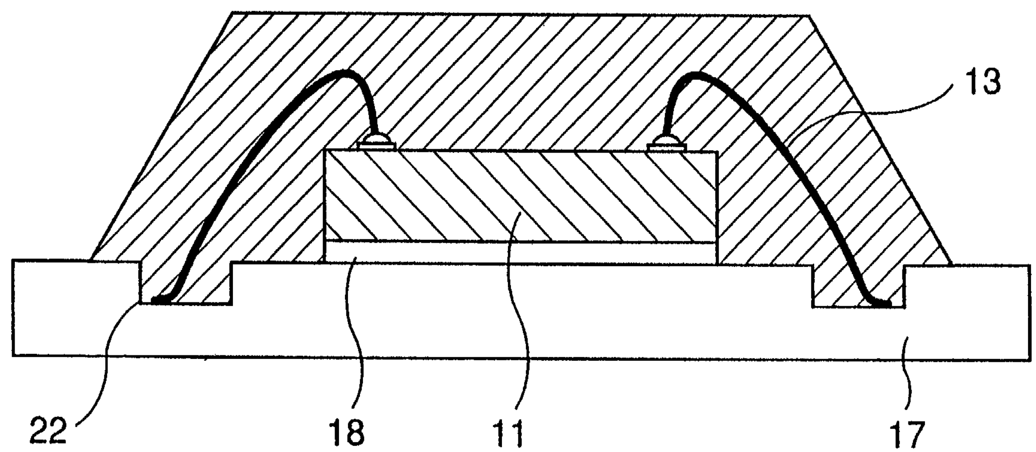


FIG.12

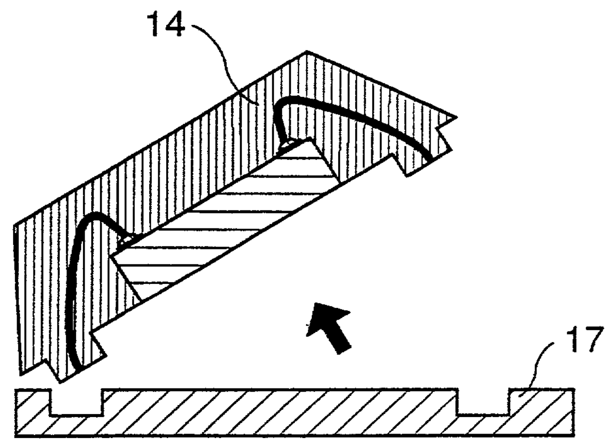


FIG.13

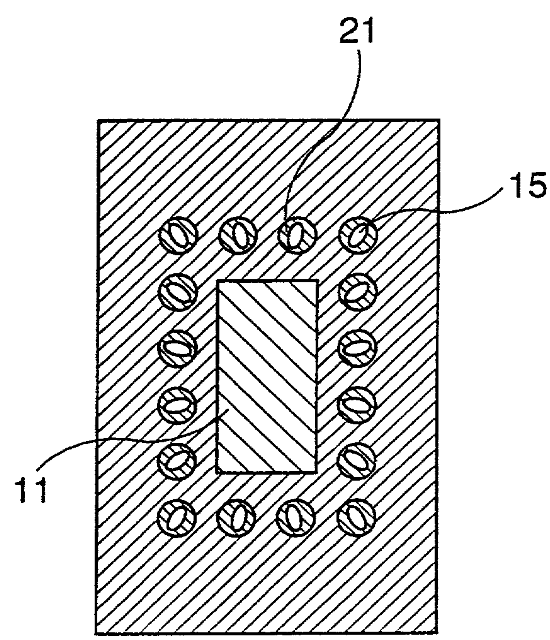


FIG.14

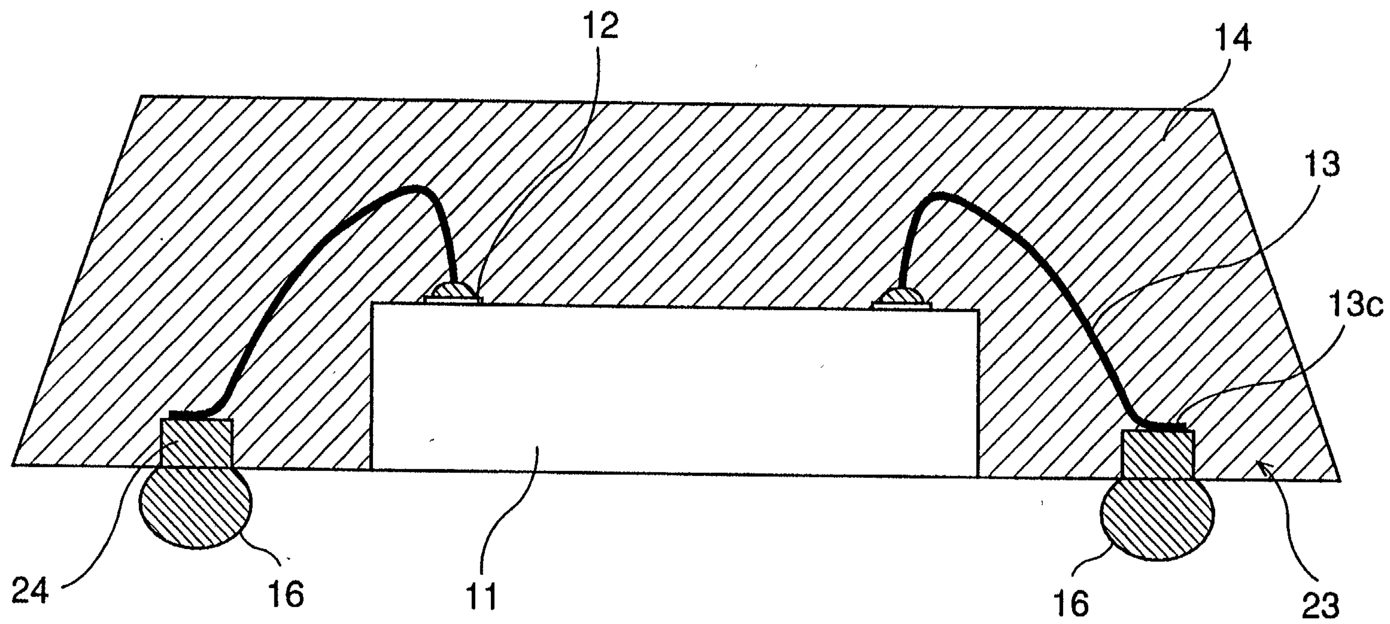


FIG.15

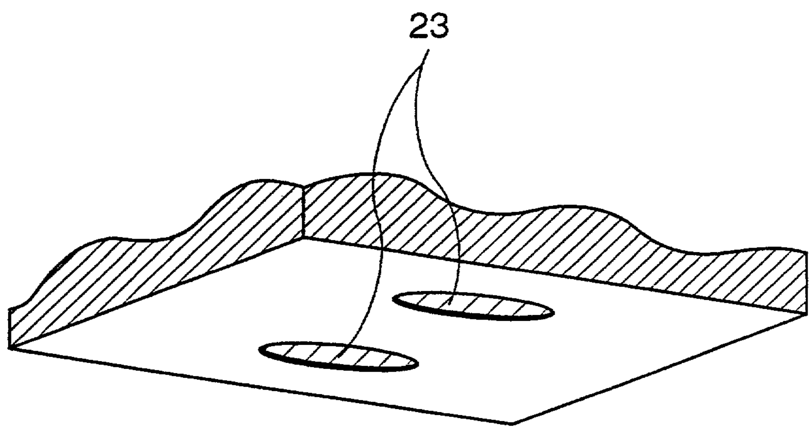


FIG.16

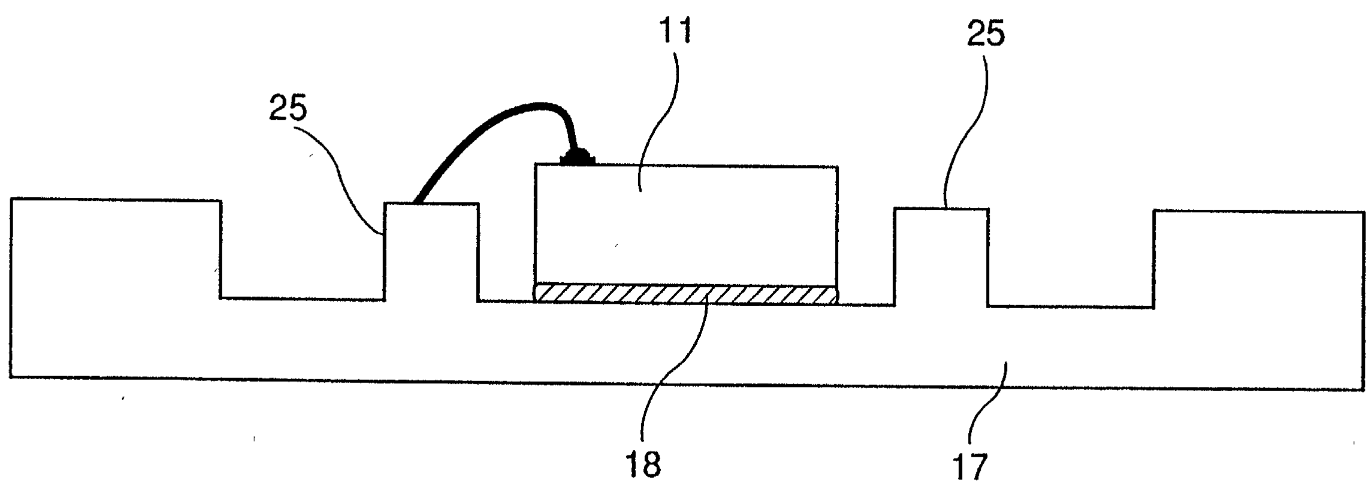


FIG.17

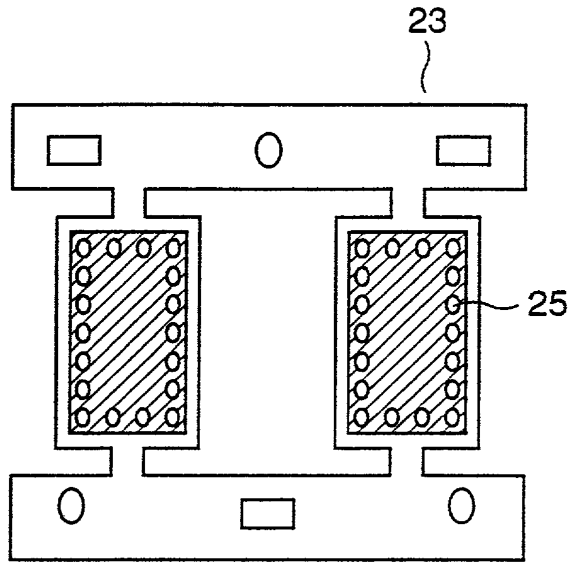


FIG.18

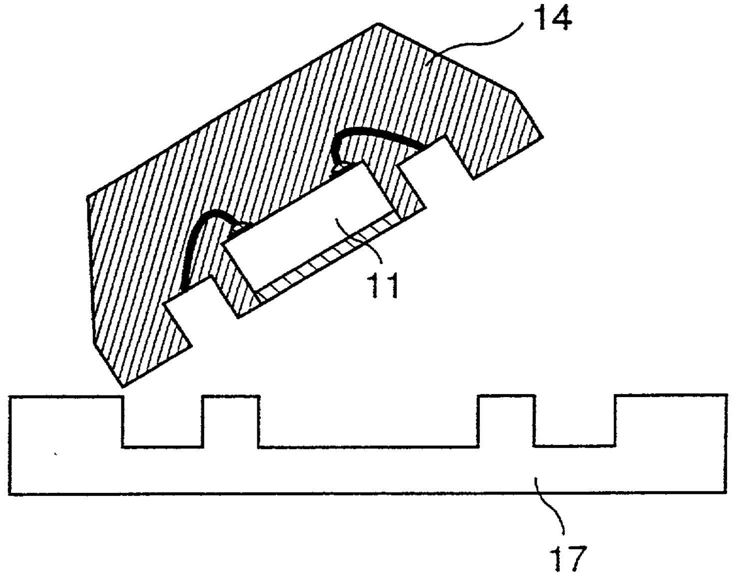


FIG.19

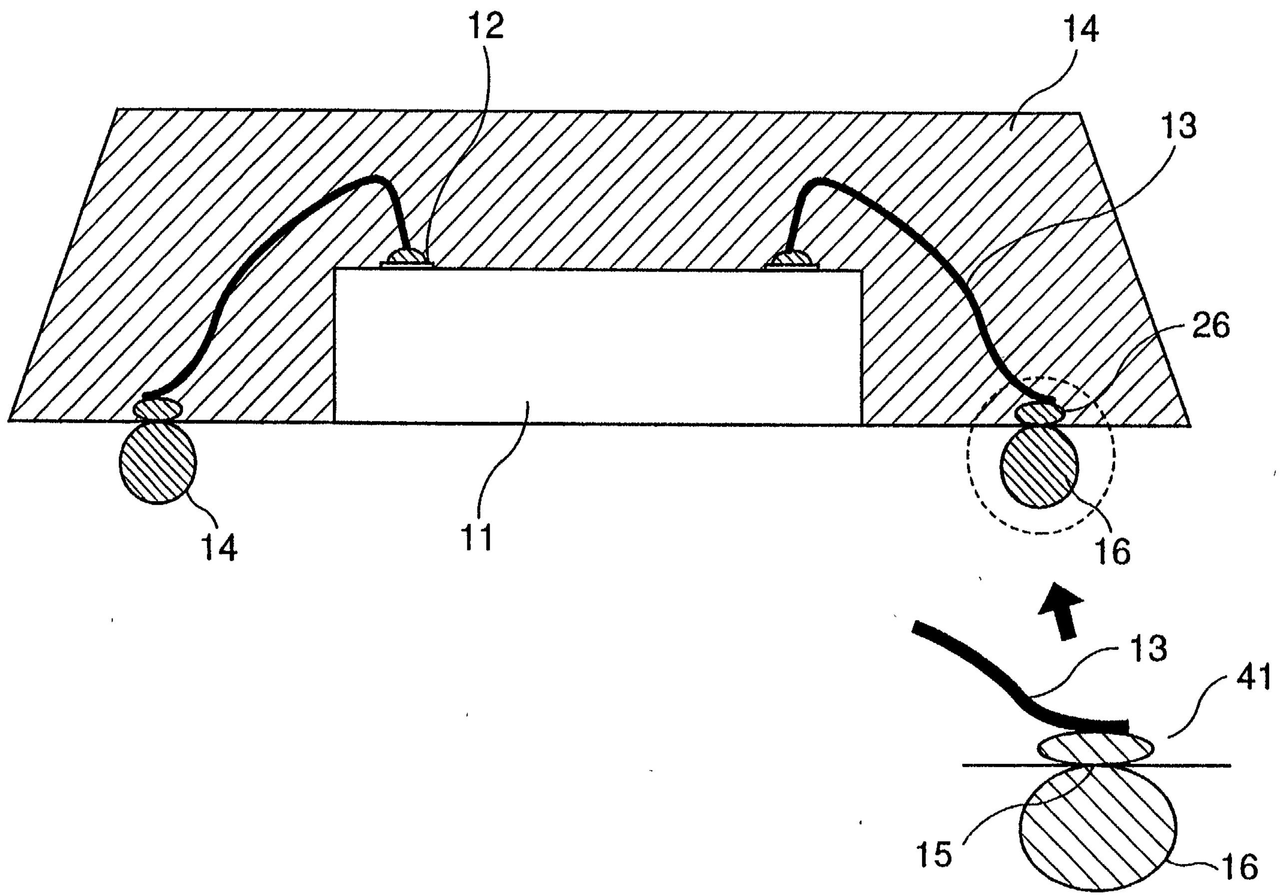


FIG.20

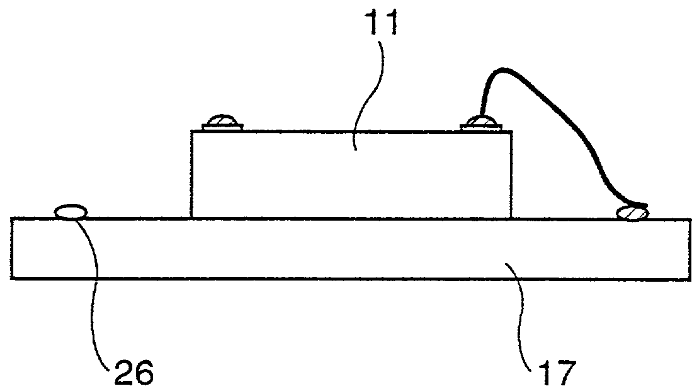


FIG.21

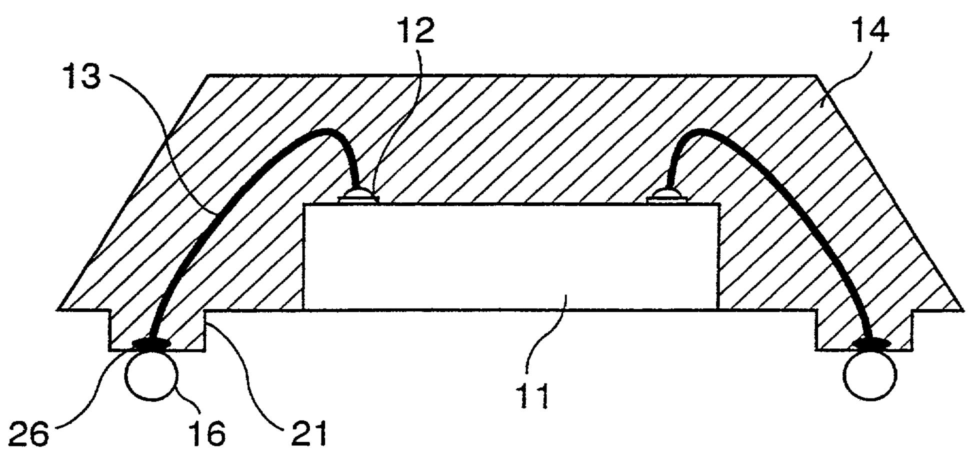


FIG.22

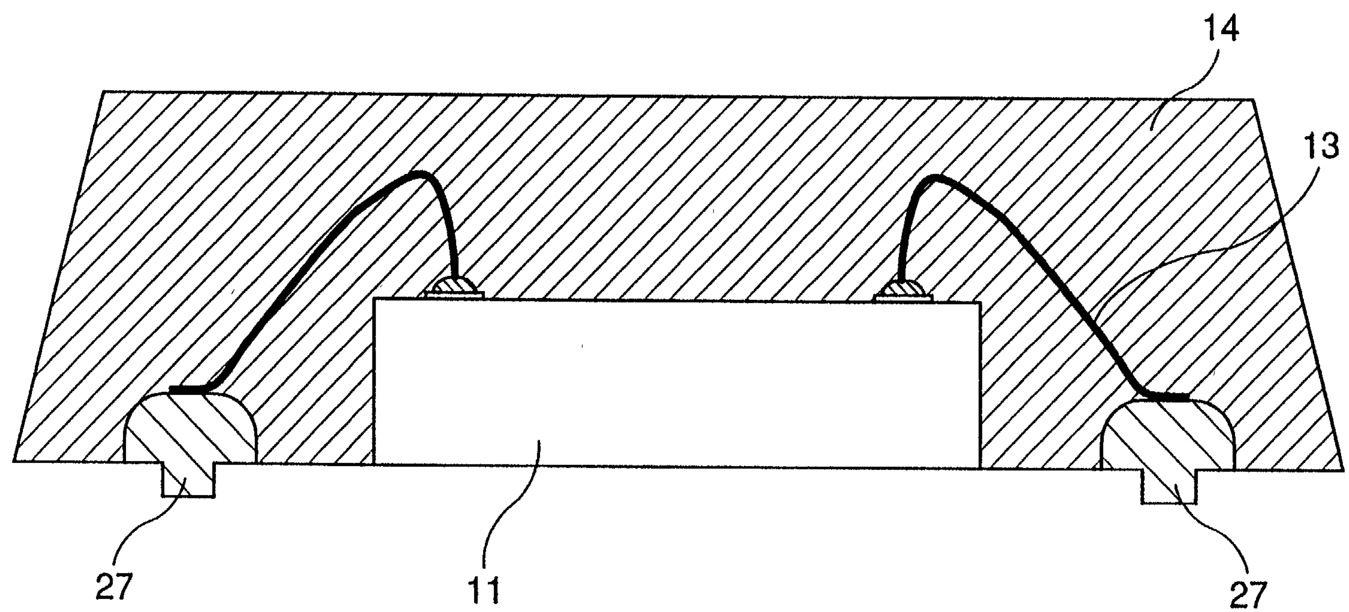


FIG.23

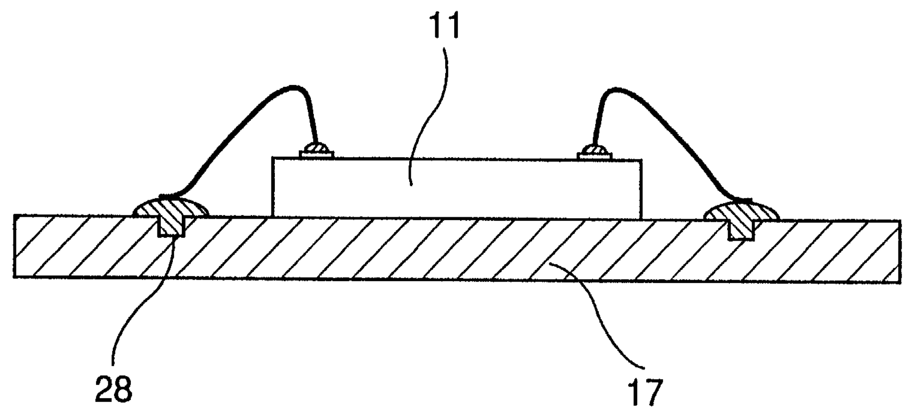


FIG.24

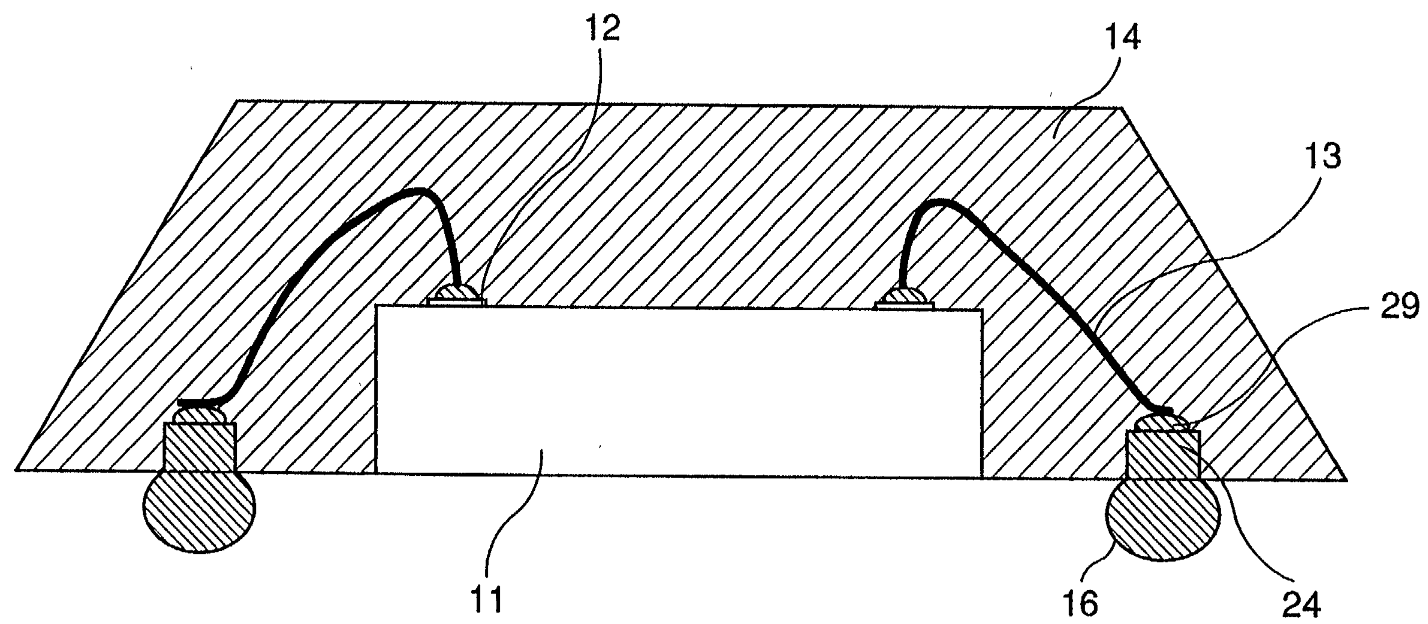


FIG.25

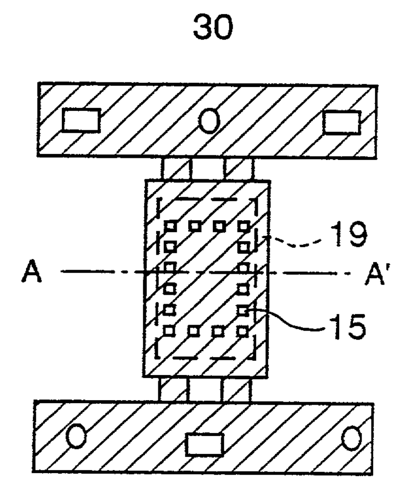


FIG.26

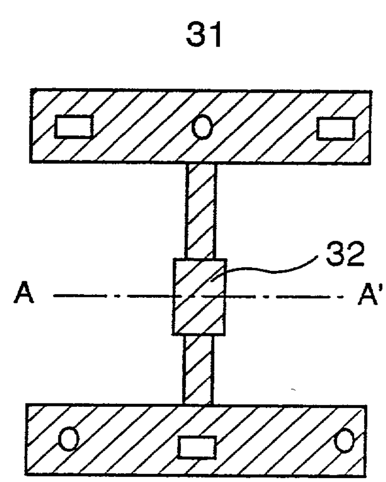


FIG.27

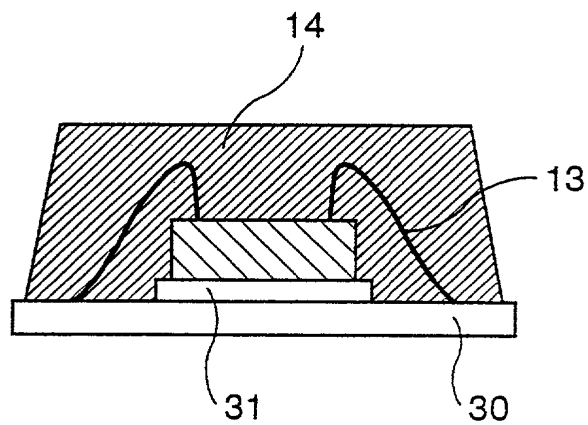


FIG.28

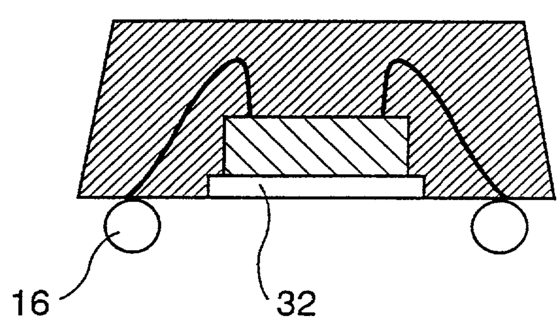


FIG.29

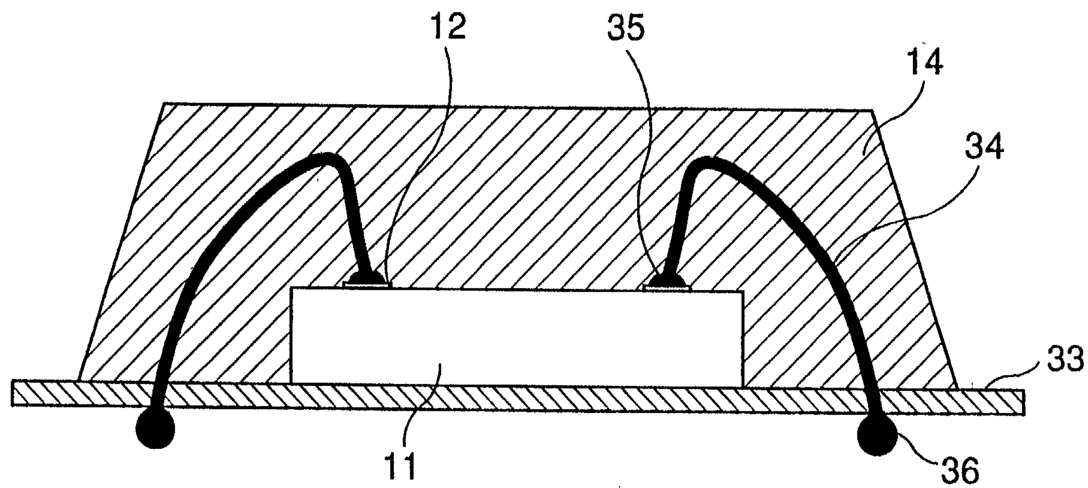


FIG.30

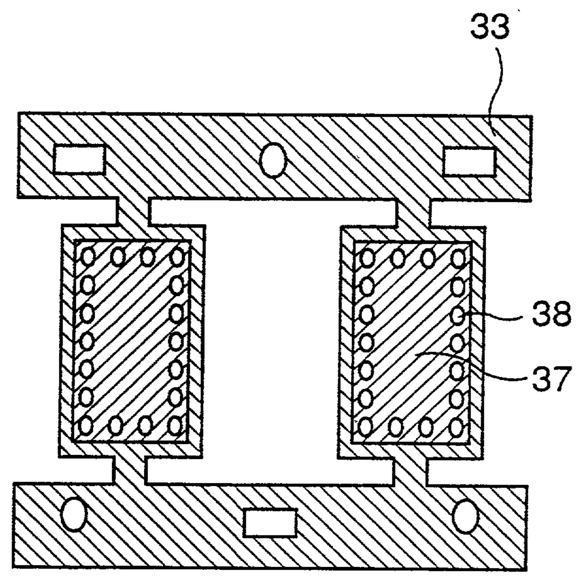


FIG.31

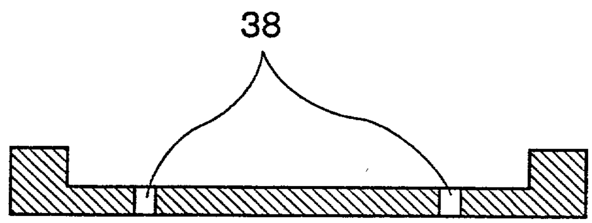


FIG. 32

110

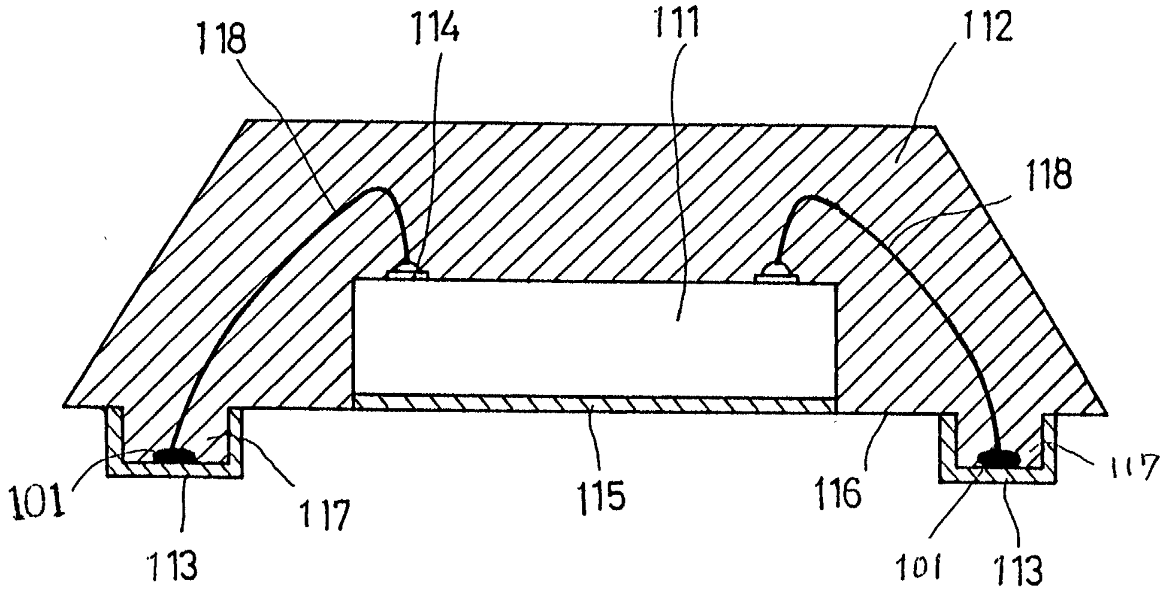
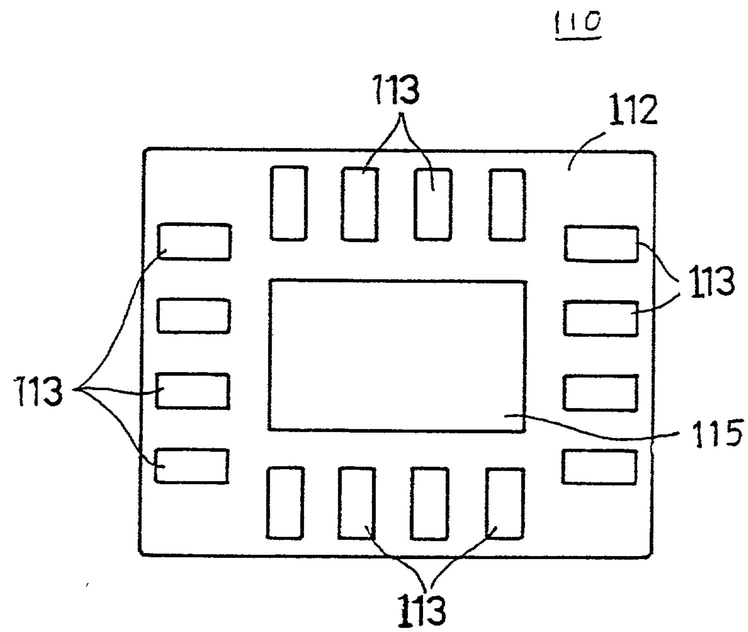


FIG. 33


110
113
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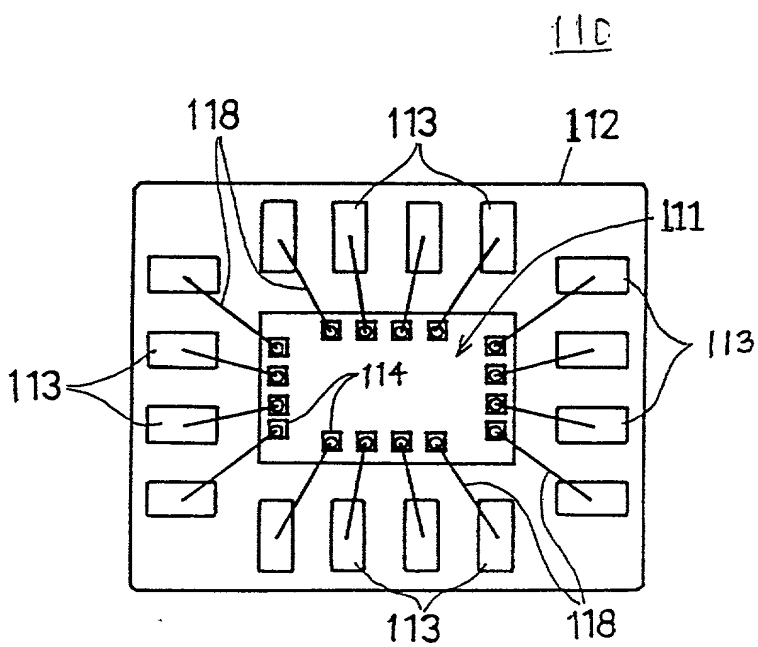
115
113

FIG. 34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118

FIG. 35

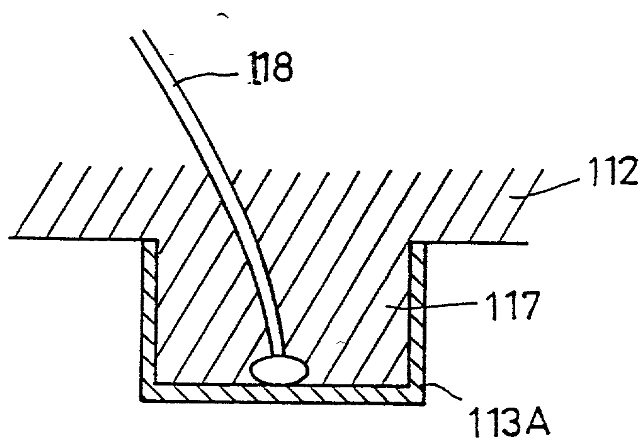


FIG. 36

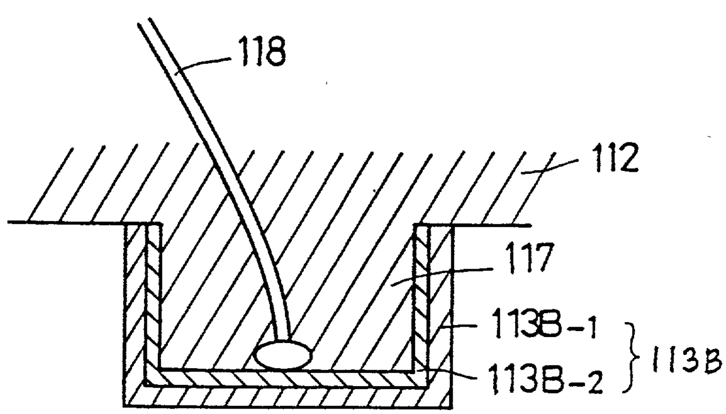
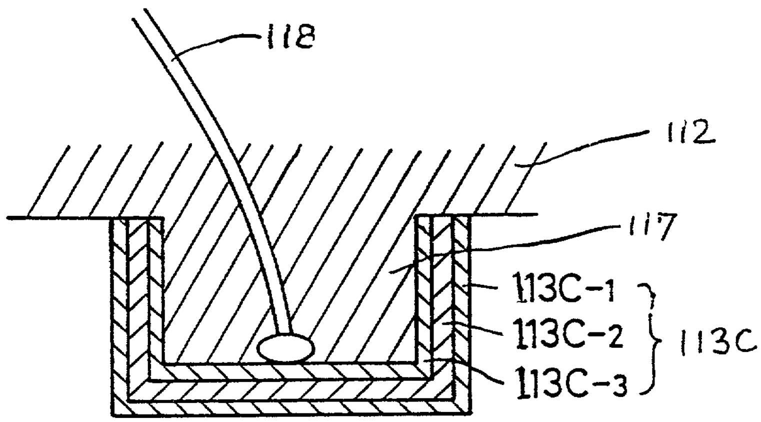


FIG. 37


118
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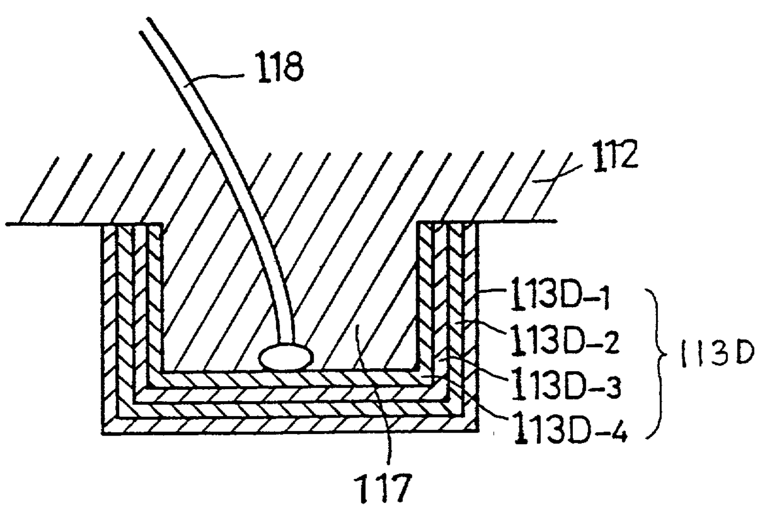
113C-1
113C-2
113C-3
113C

FIG. 38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117

FIG. 39

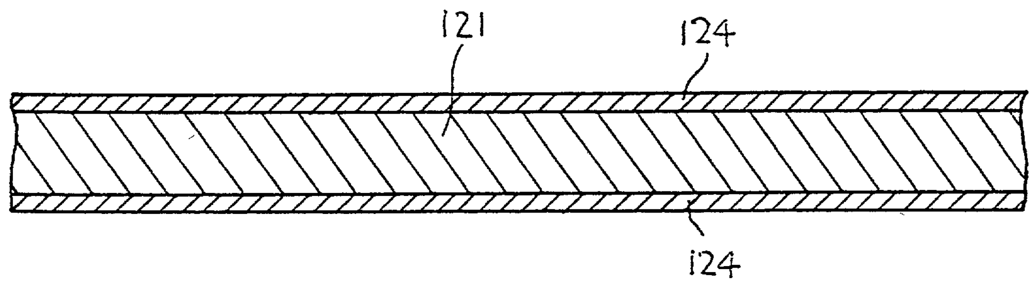


FIG. 40

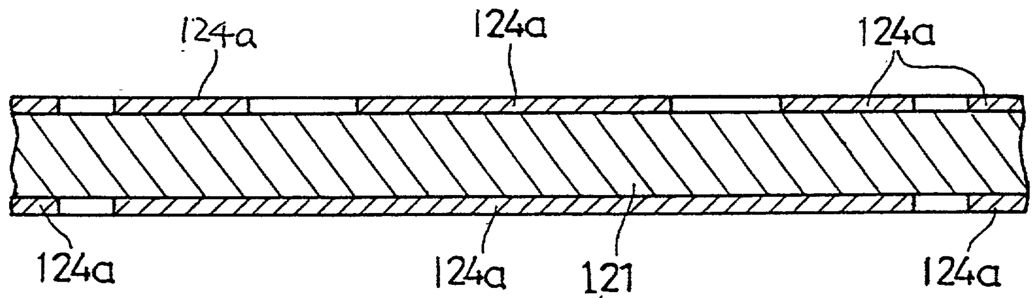


FIG. 41

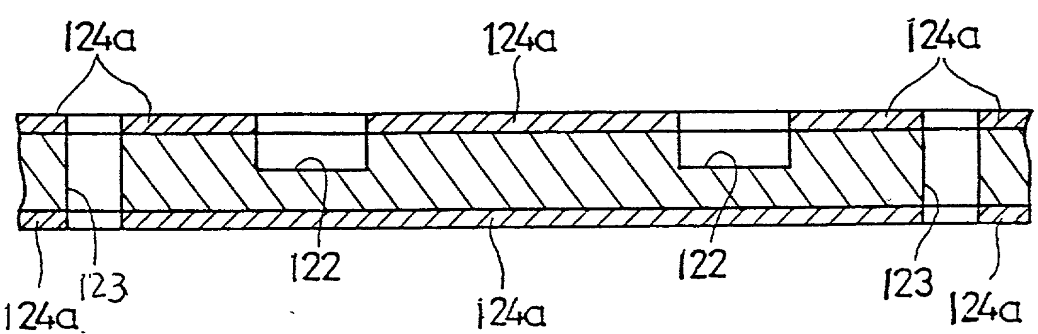


FIG. 42A

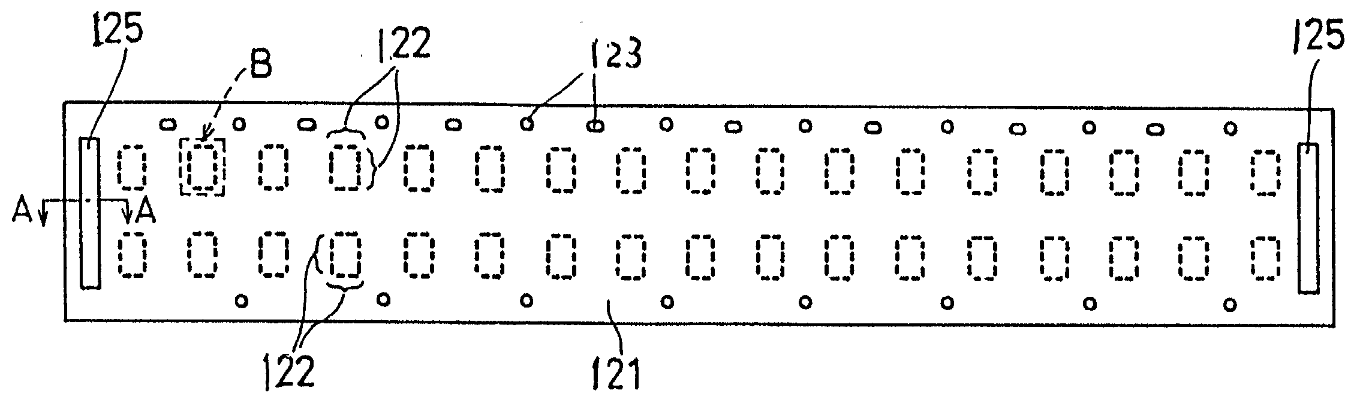


FIG. 42B

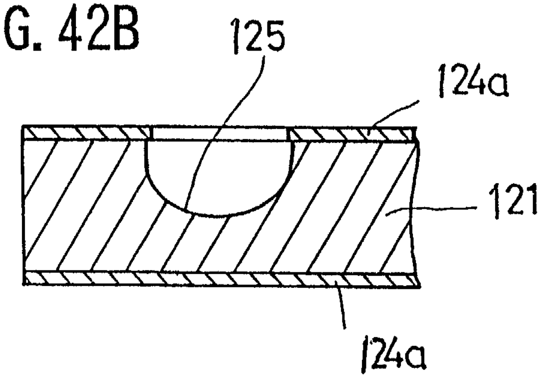
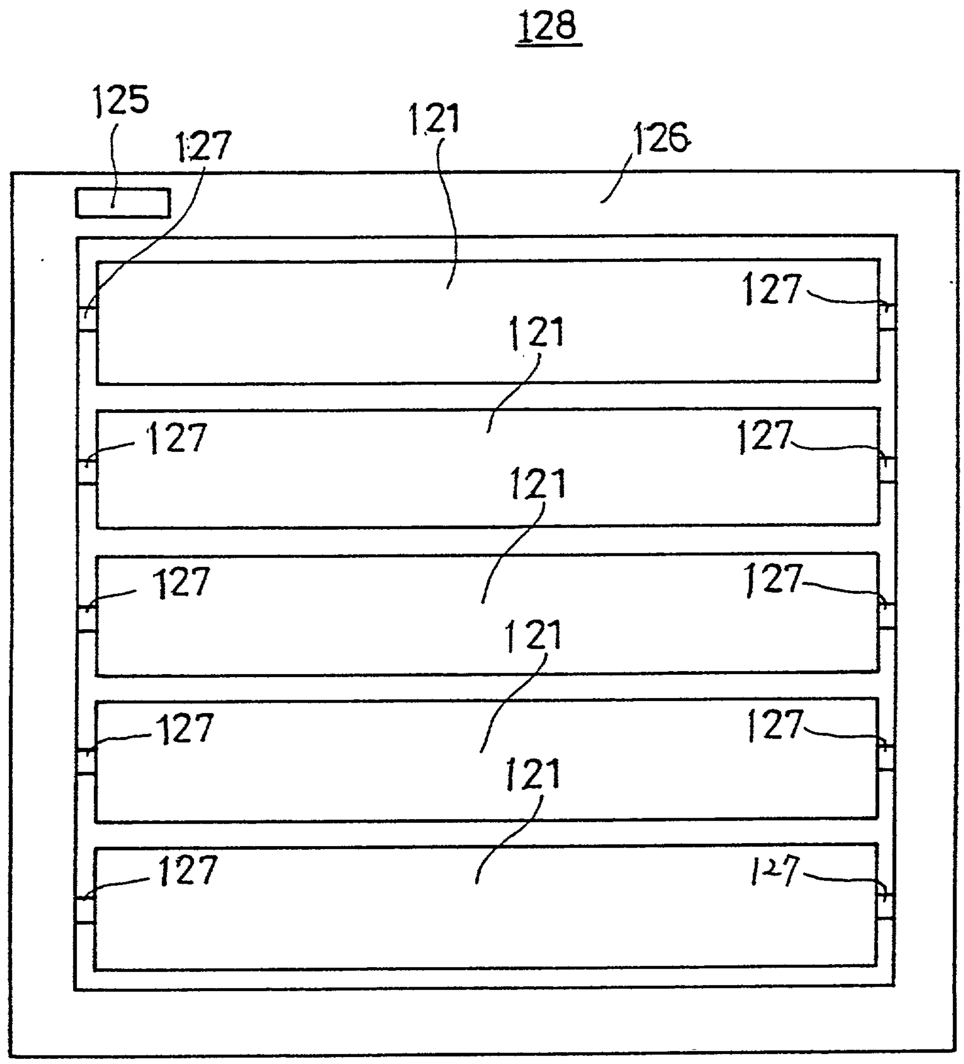


FIG. 43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127
121
127
127

FIG. 44

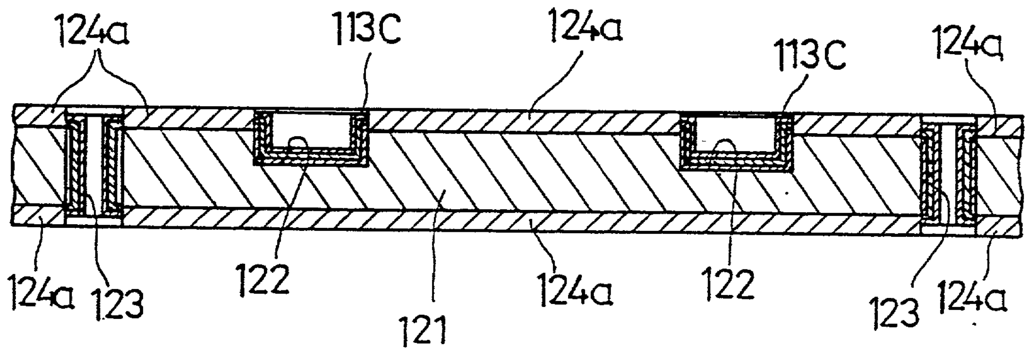

124a
113C
124a
113C
124a
124a
123
122
121
124a
122
123
124a

FIG. 45

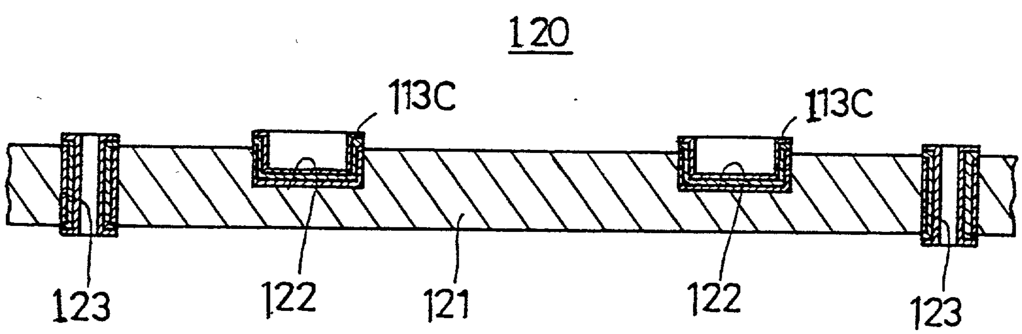

120
113C
113C
123
122
121
122
123

FIG. 46

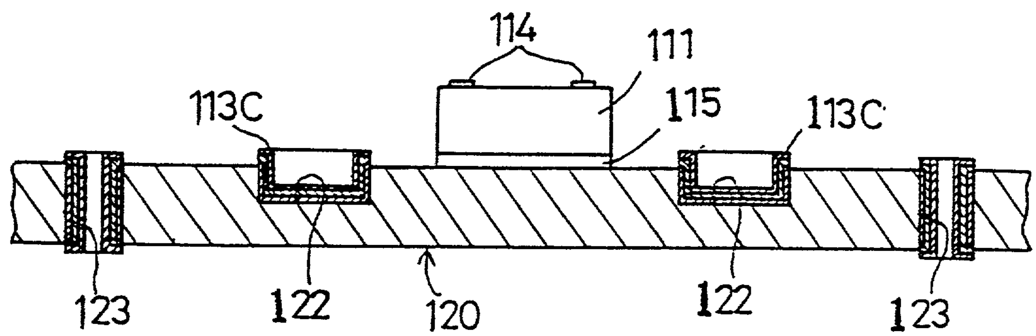

114
111
113C
115
113C
123
122
120
122
123

FIG. 47

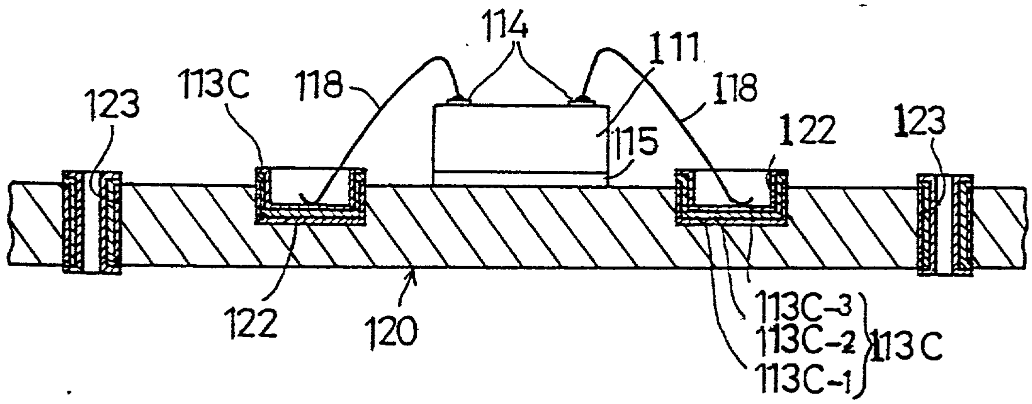

114
111
123
113C
118
118
115
122
123
122
120
113C-3
113C-2
113C-1
113C

FIG. 48

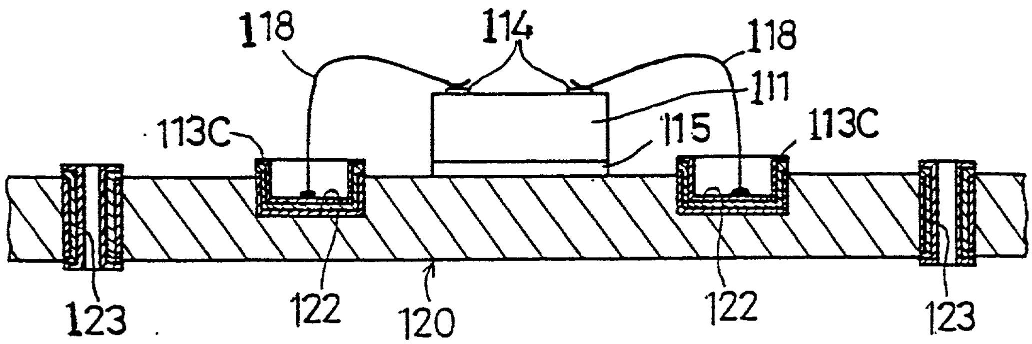


FIG. 49

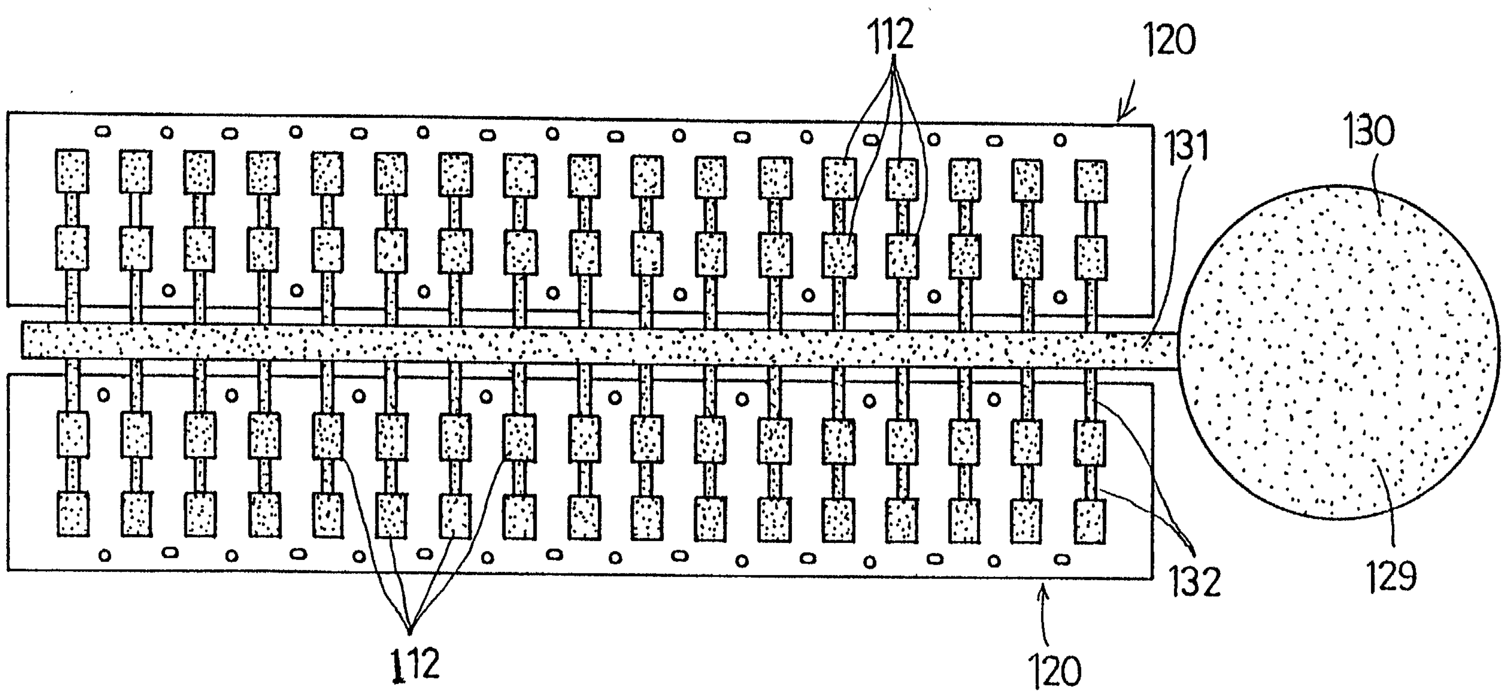


FIG. 50

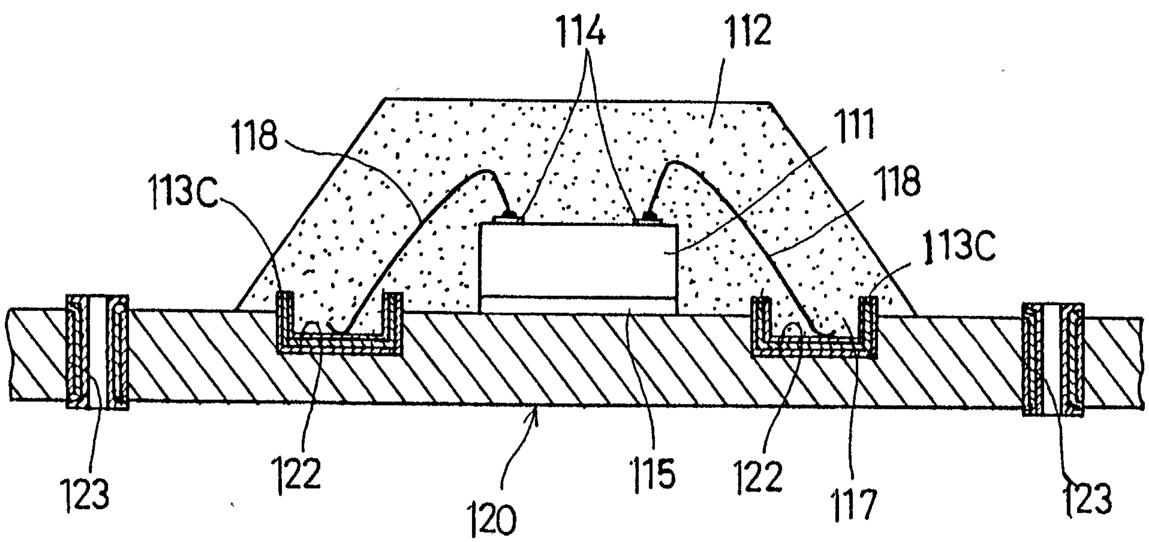


FIG. 51A

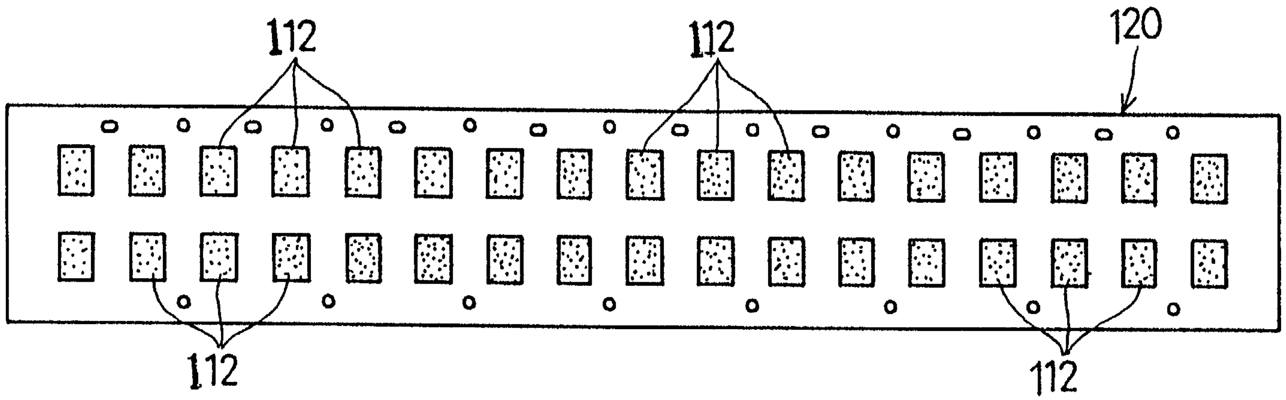


FIG. 51B

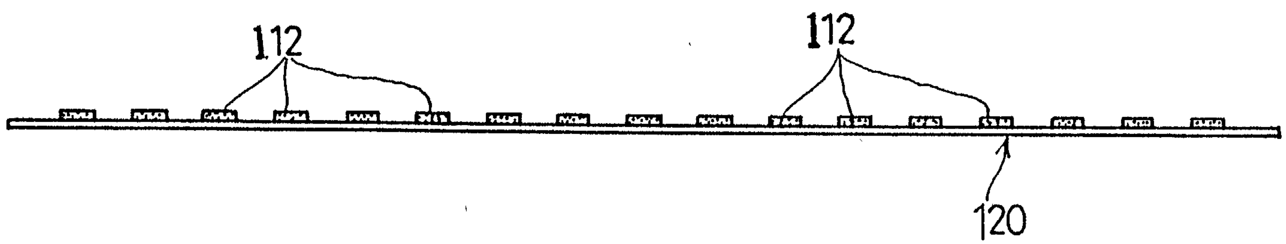


FIG. 52A

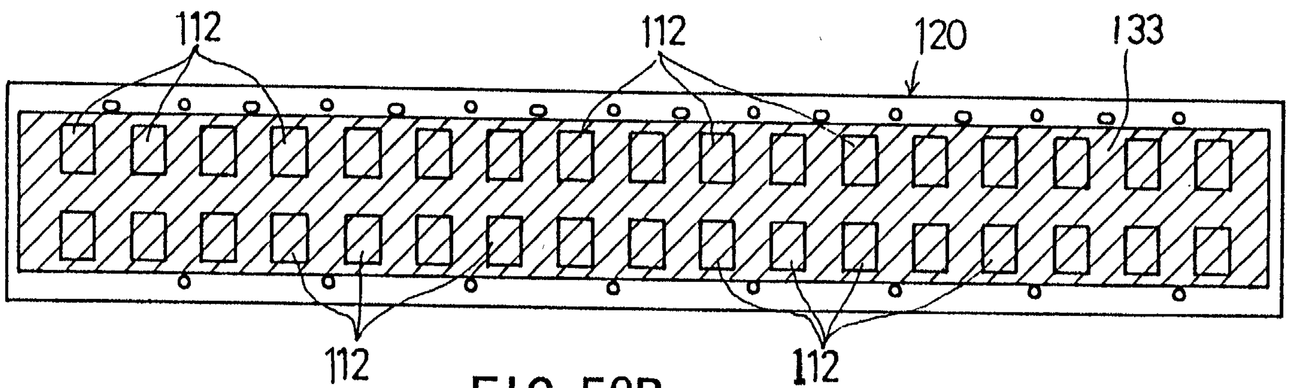


FIG. 52B

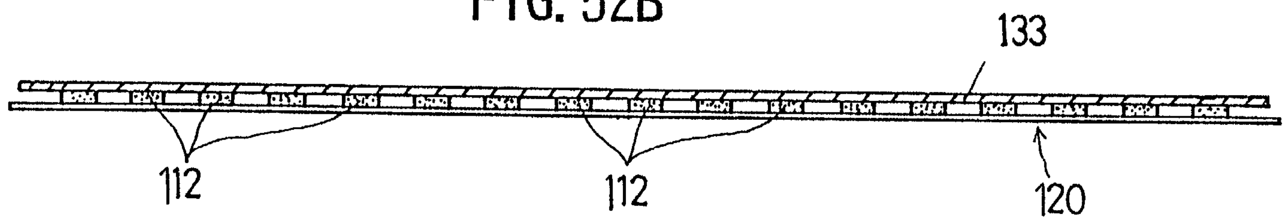


FIG. 53

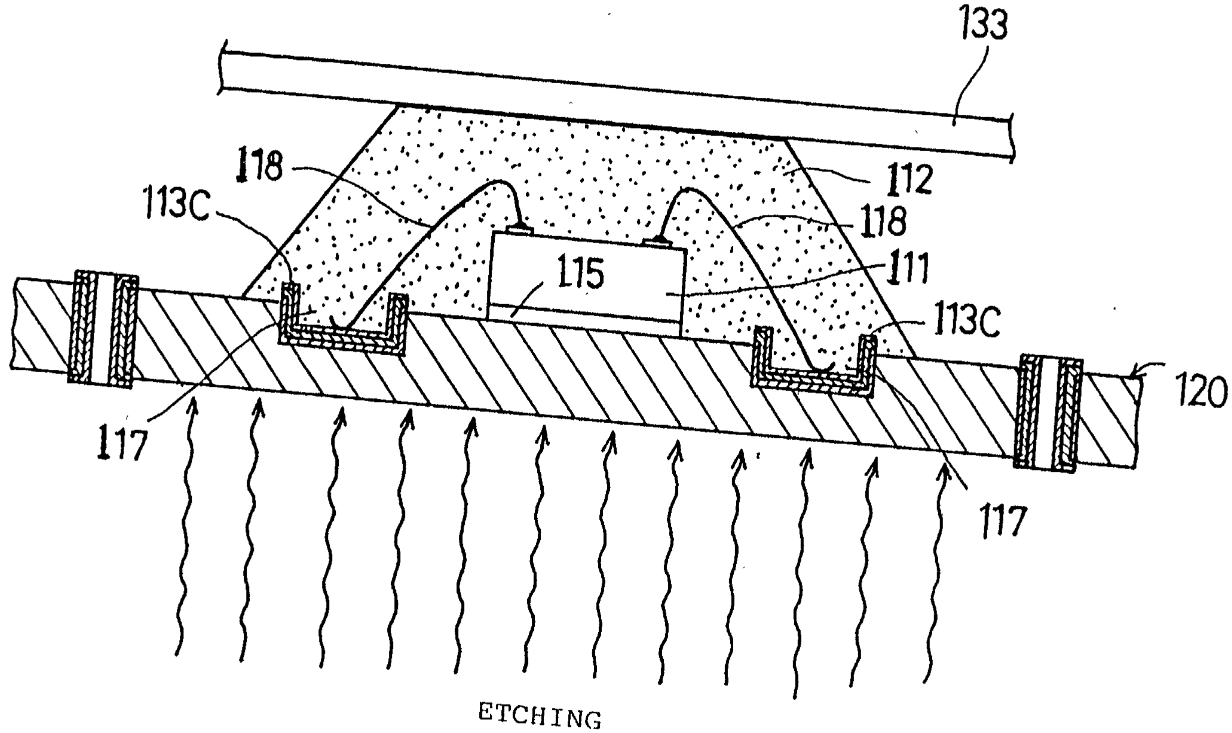


FIG. 54A

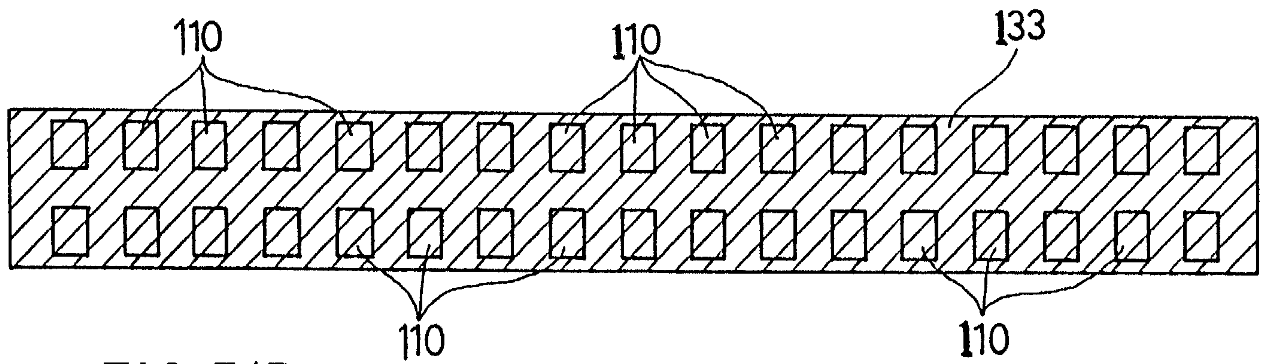


FIG. 54B

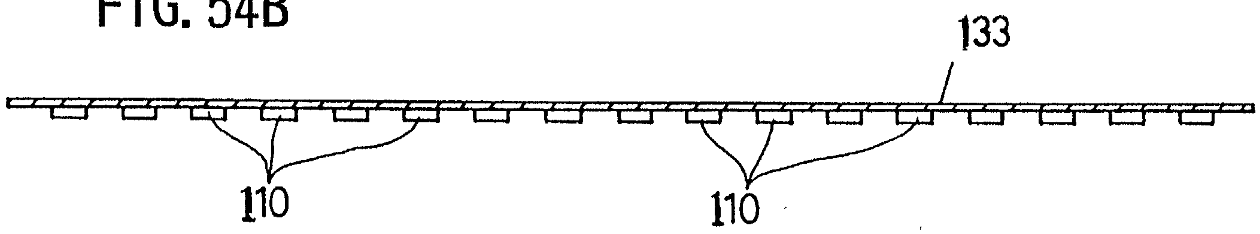


FIG. 55A

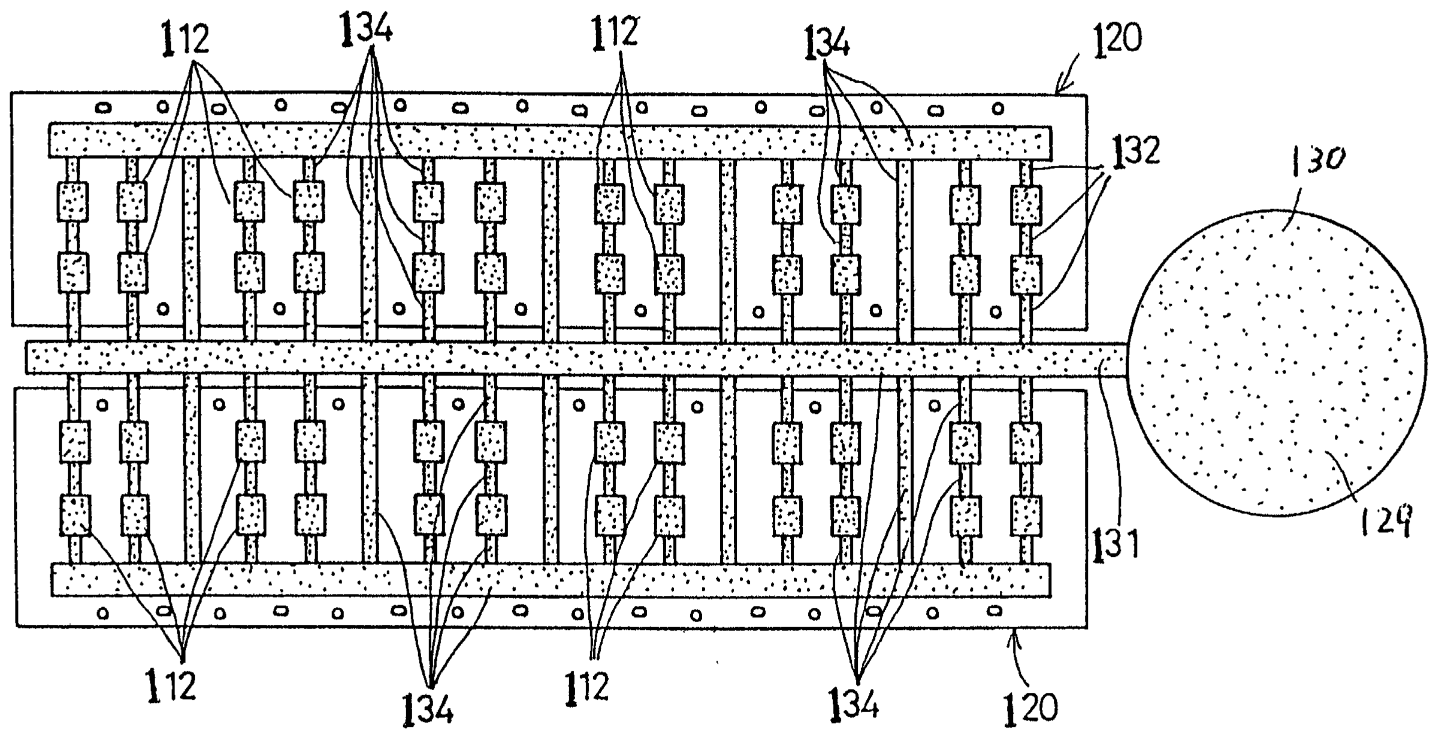


FIG. 55B

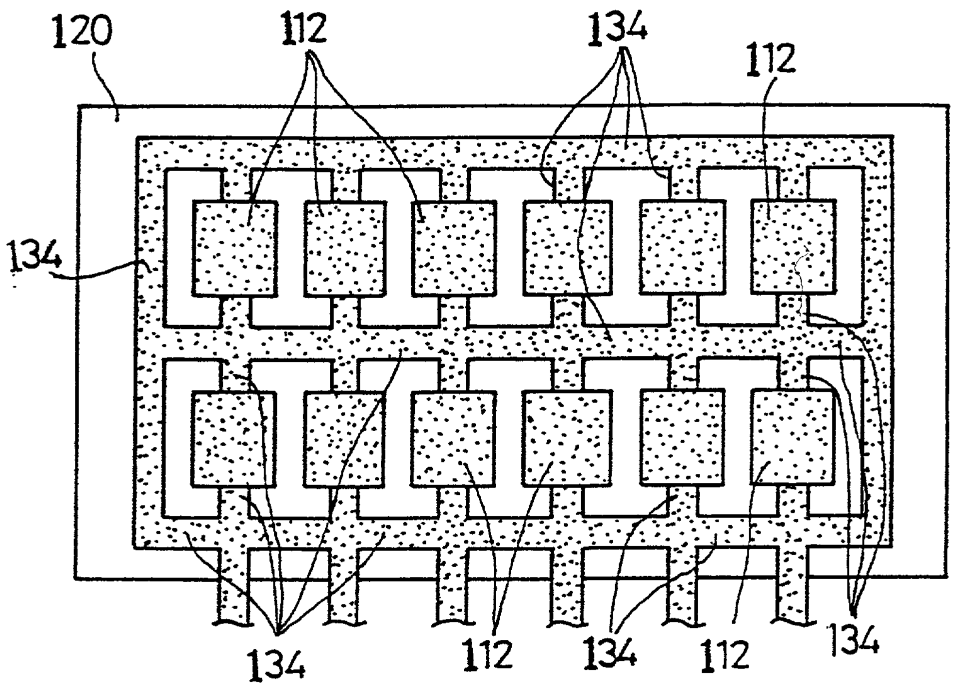


FIG. 55C

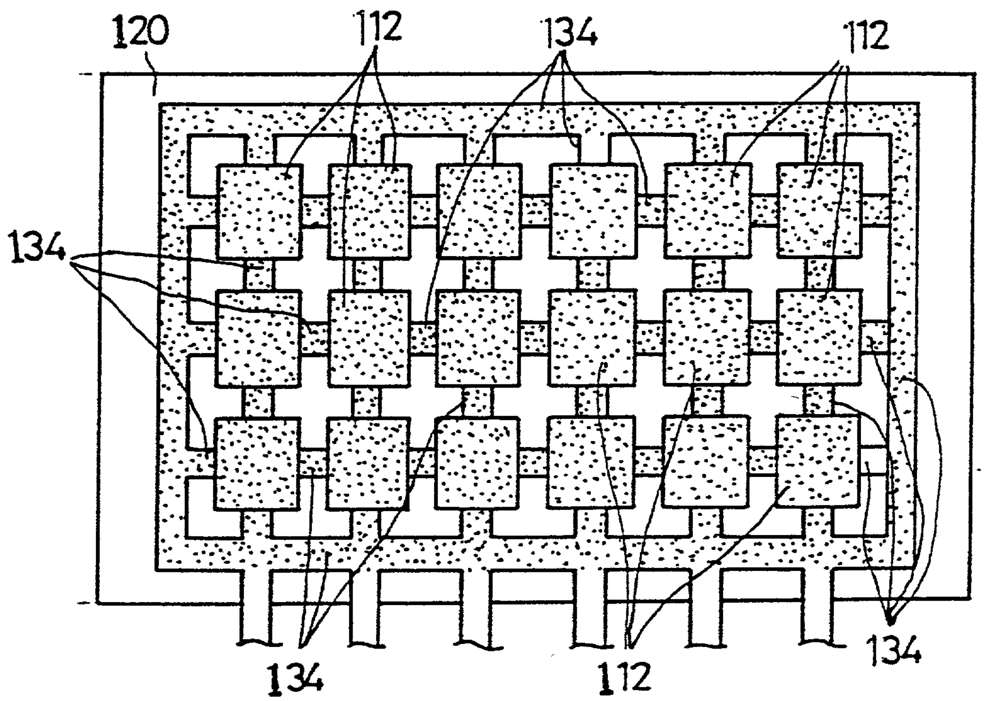


FIG. 56

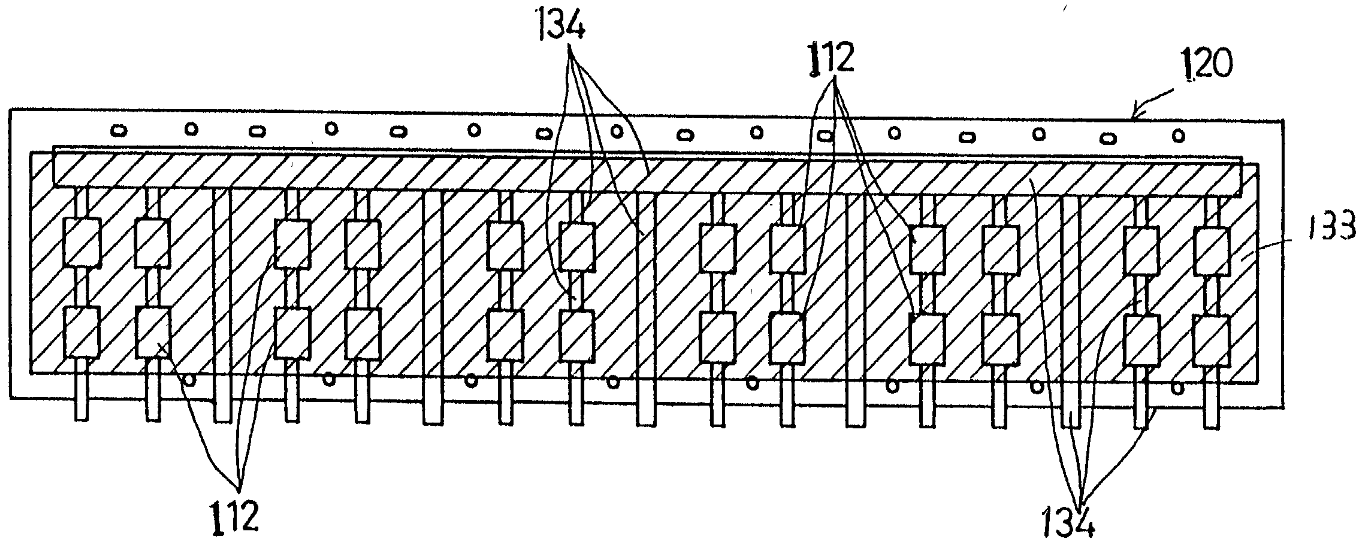


FIG. 57A

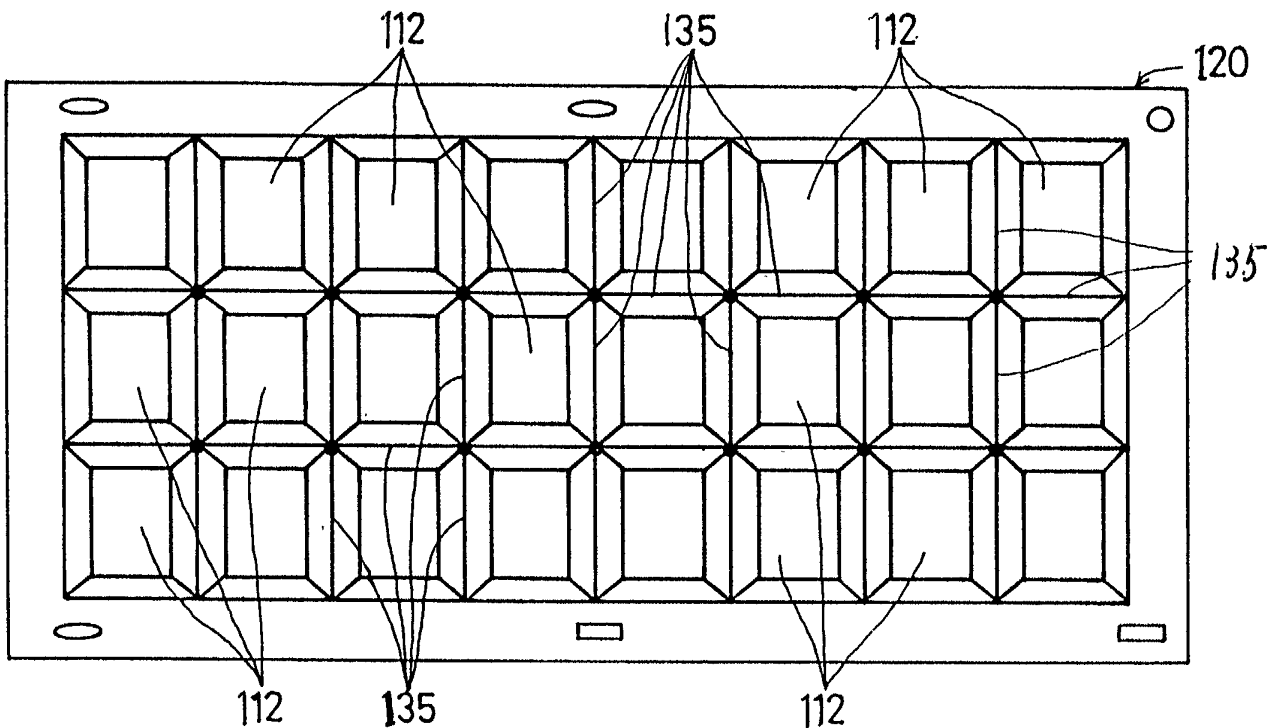


FIG. 57B

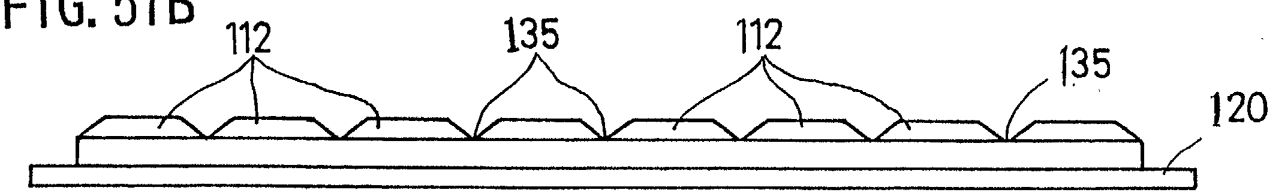


FIG. 58

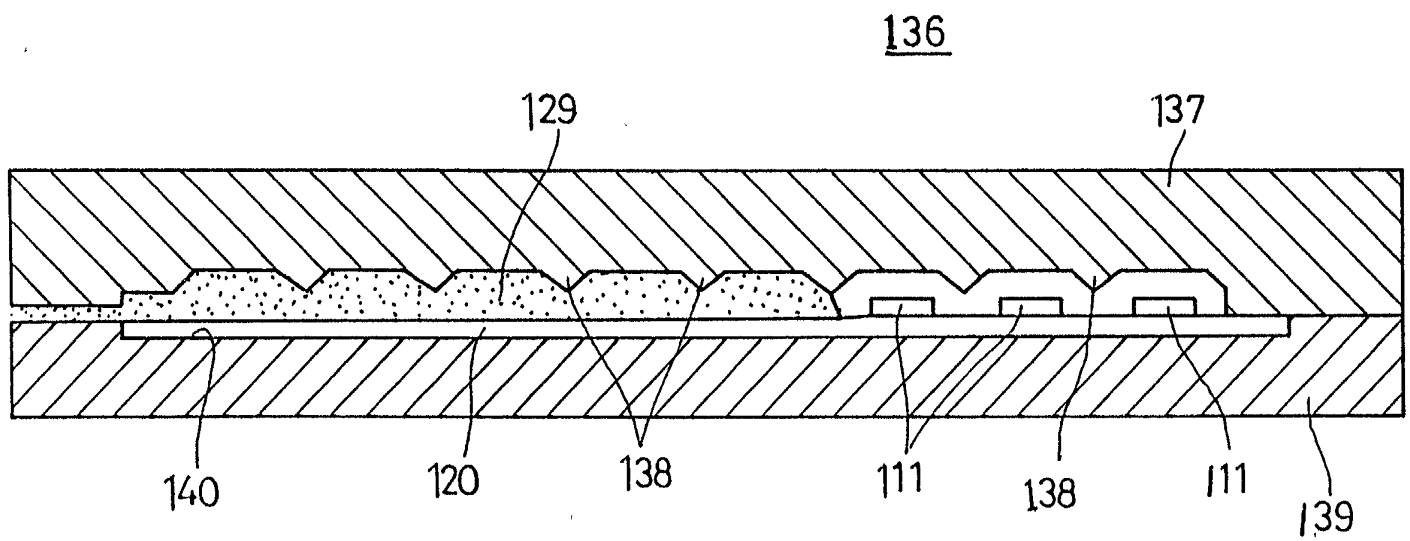


FIG. 59

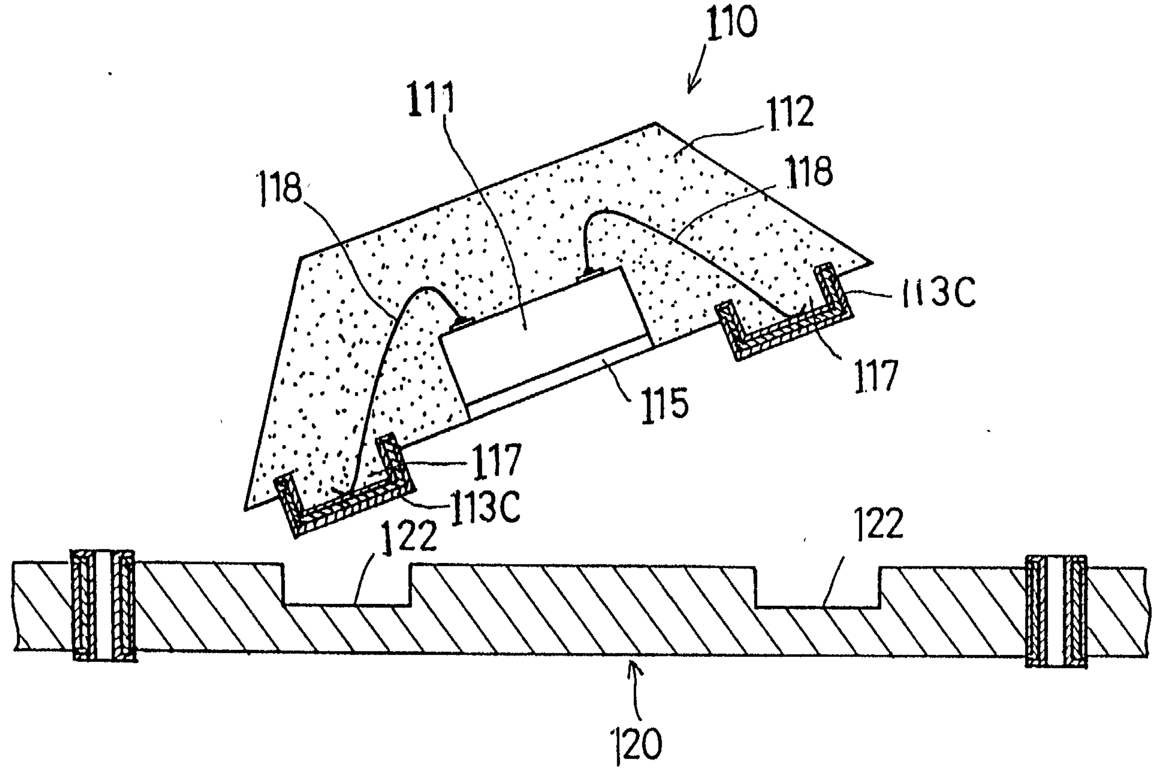


FIG. 60

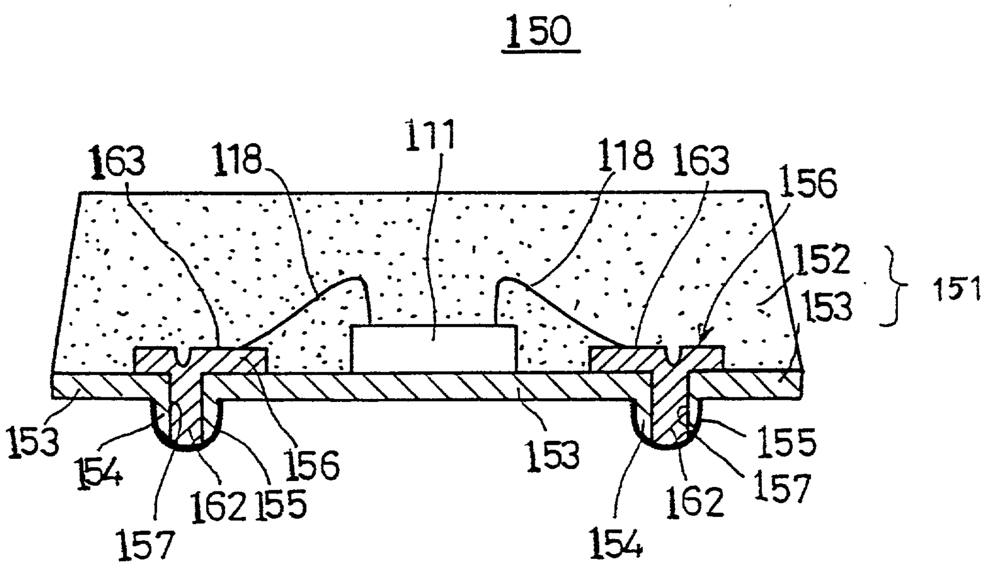


FIG. 61

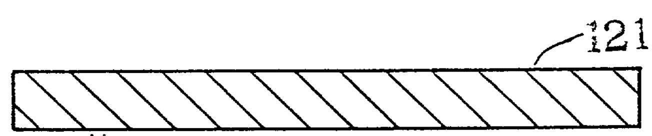


FIG. 62

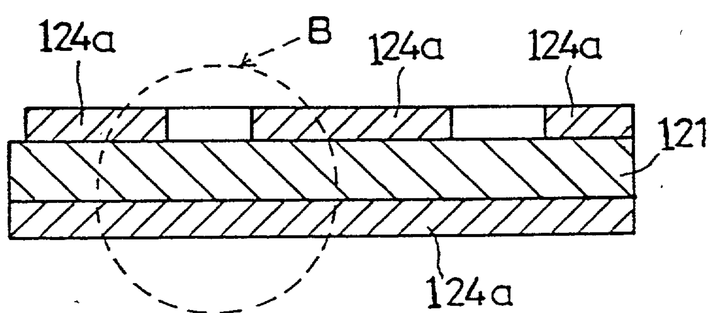


FIG. 63

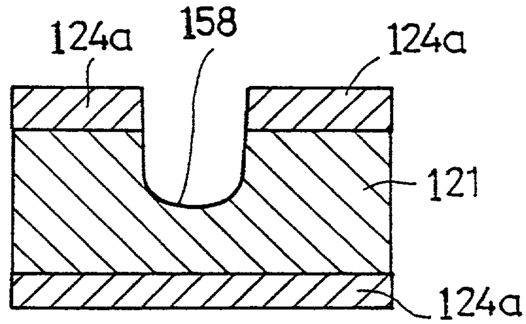


FIG. 64

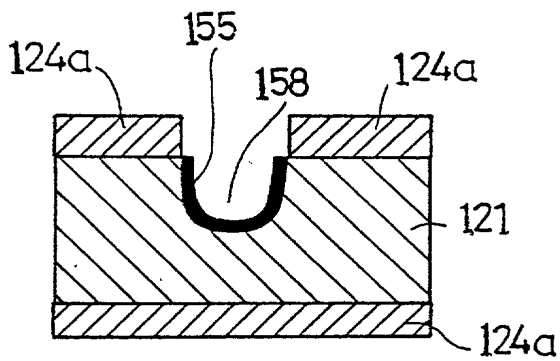


FIG. 65

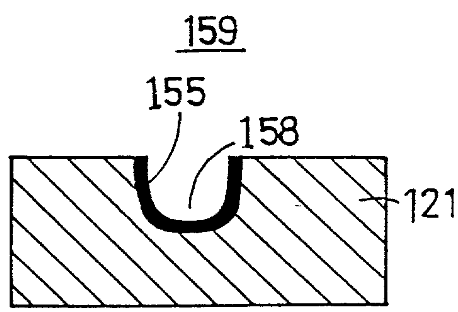


FIG. 66

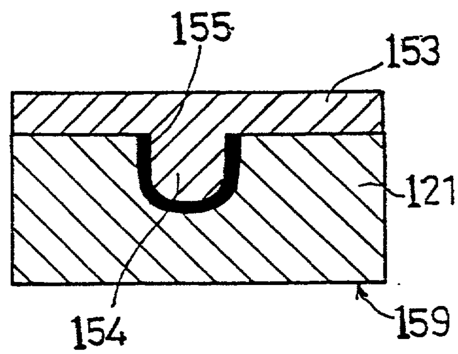


FIG. 67

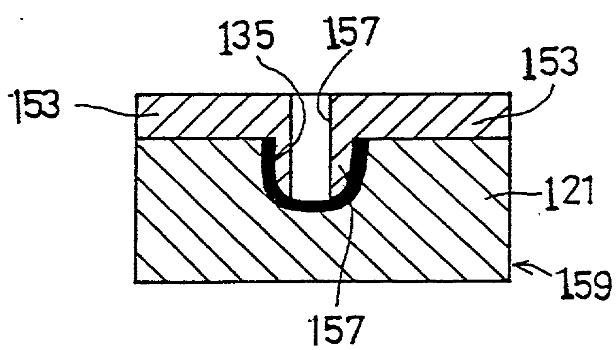


FIG. 68

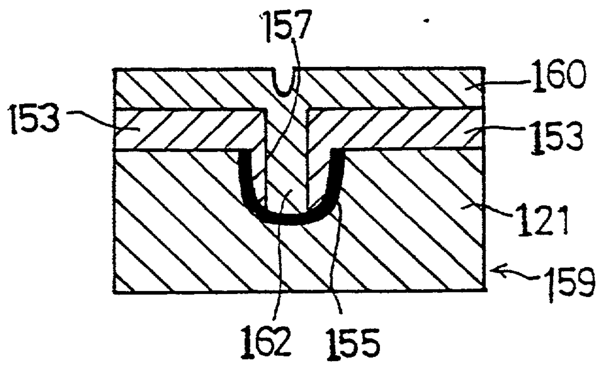
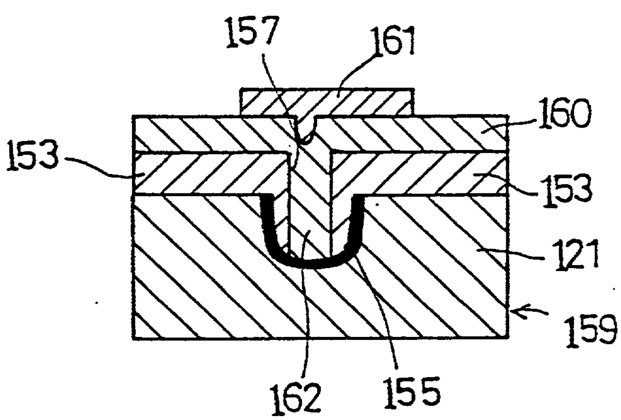

157
160
153
153
121
159
162
155

FIG. 69


157
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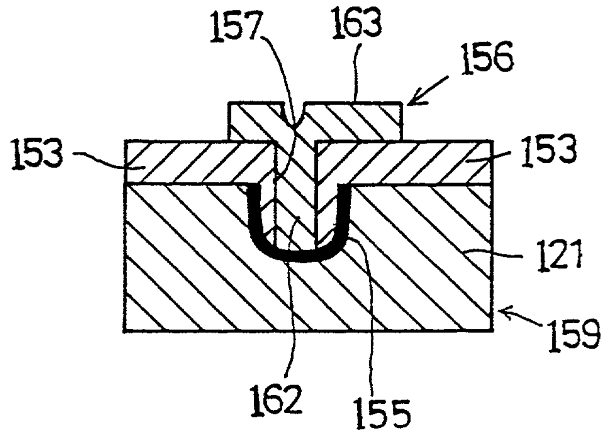
153
121
159
162
155

FIG. 70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156
153
153
121
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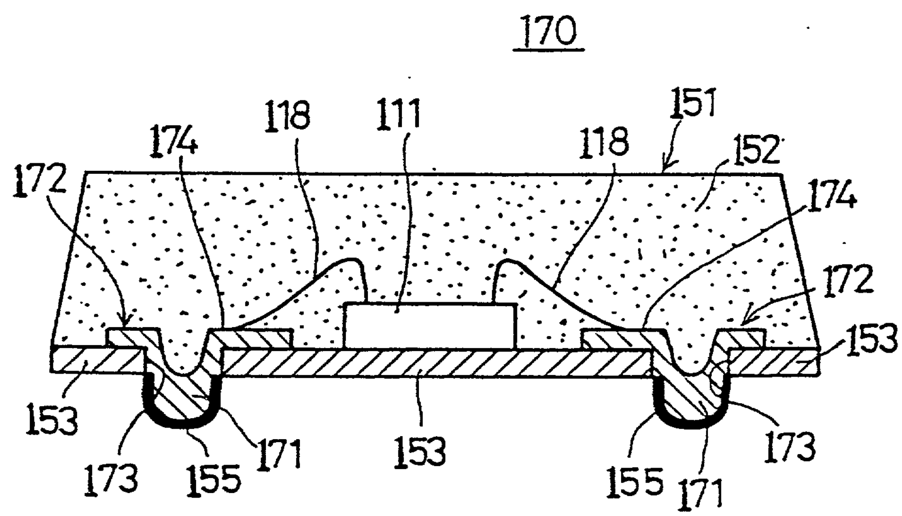
162
155

FIG. 71


170
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118
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153
153
153
173
155
171
155
171
173

FIG. 72

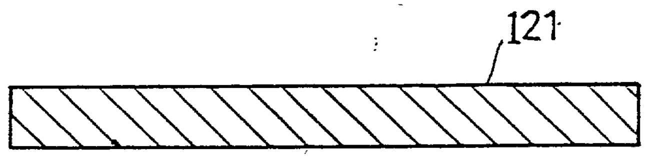


FIG. 73

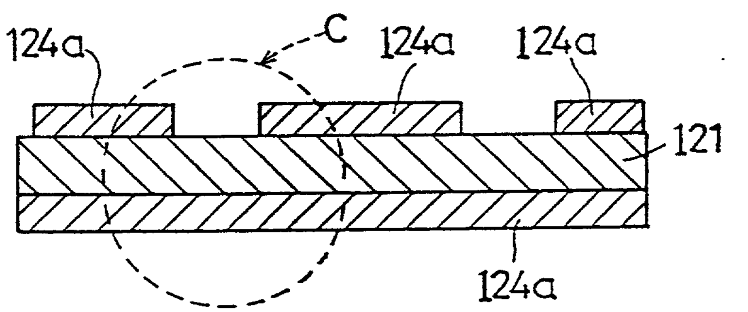


FIG. 74

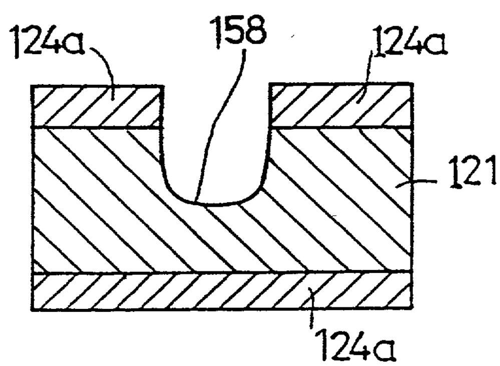


FIG. 75

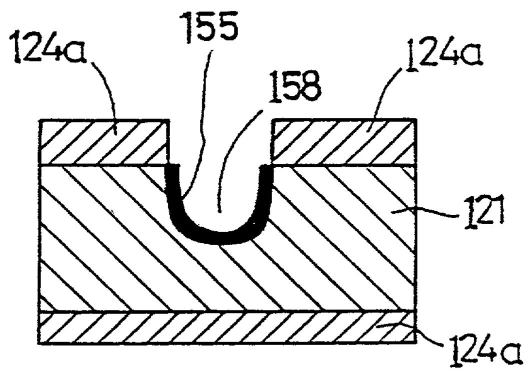


FIG. 76

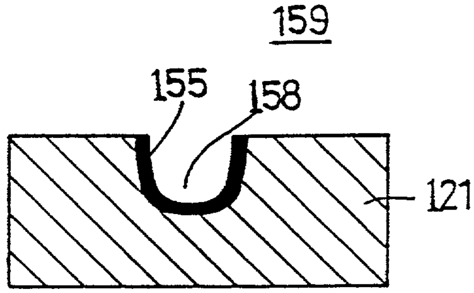


FIG. 77

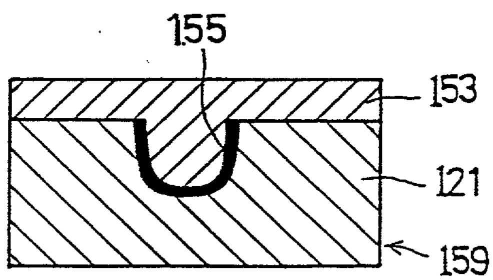


FIG. 78

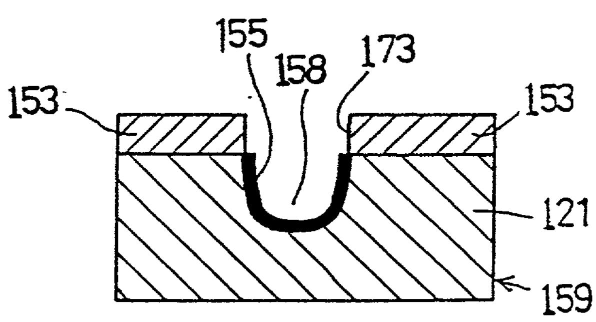


FIG. 79

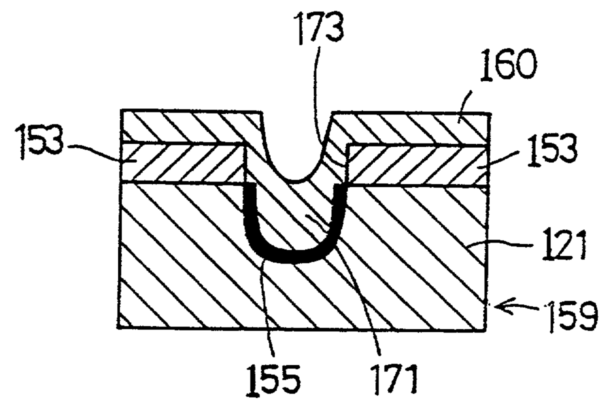
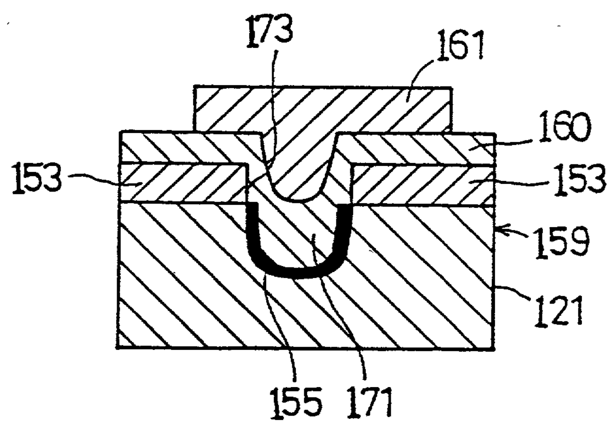

173
160
153
153
121
159
155
171

FIG. 80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161
160
153
153
159
121
155
171

FIG. 81

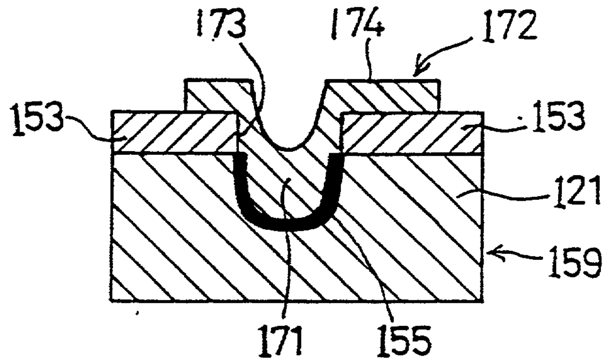
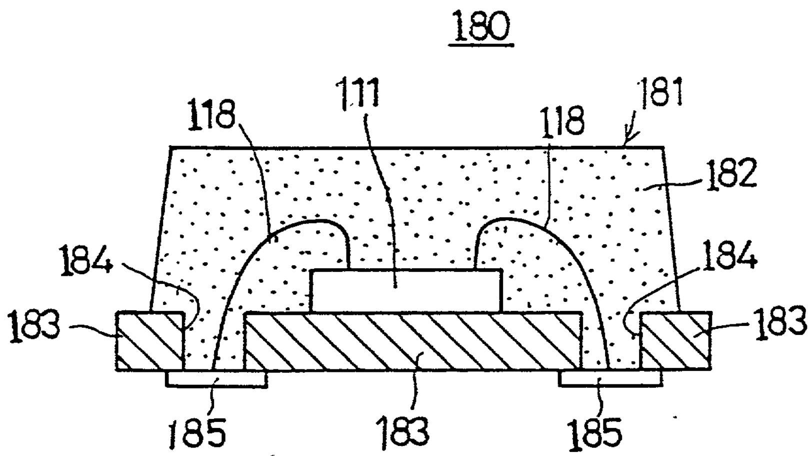

173
174
172
153
153
121
159
171
155

FIG. 82


180
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118
182
184
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183
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185
183
185

FIG. 83

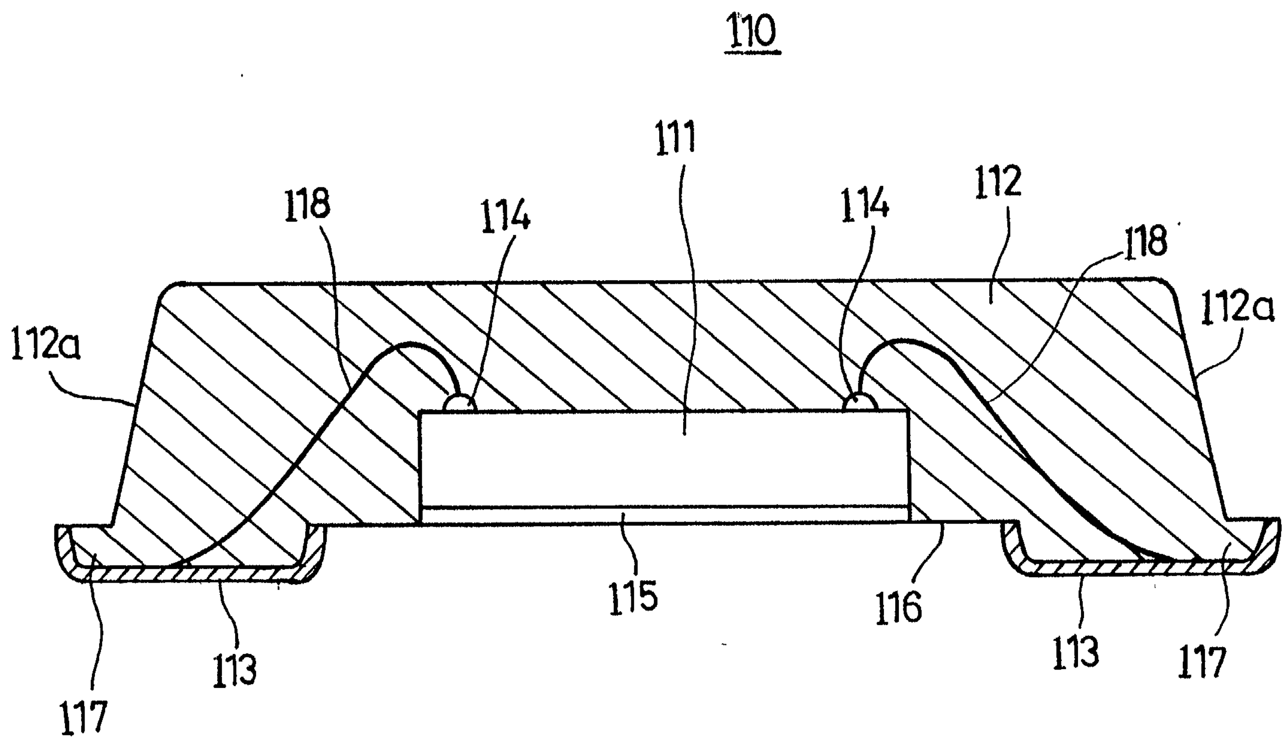


FIG. 84A

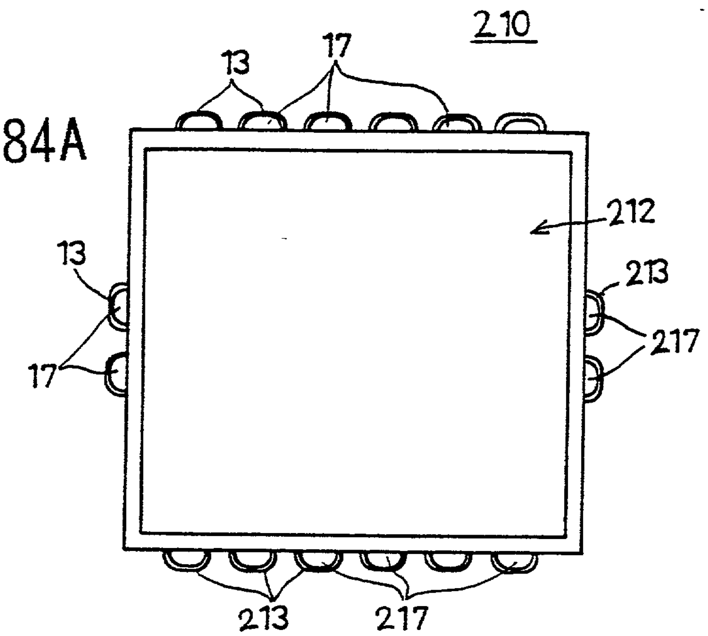


FIG. 84B

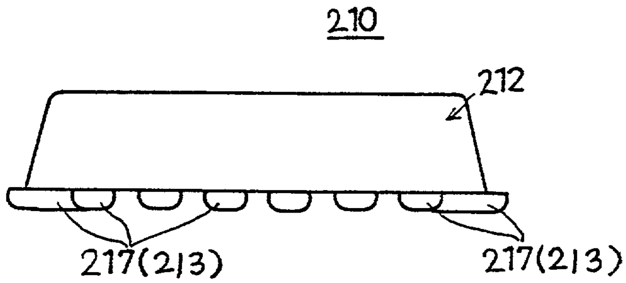


FIG. 84C

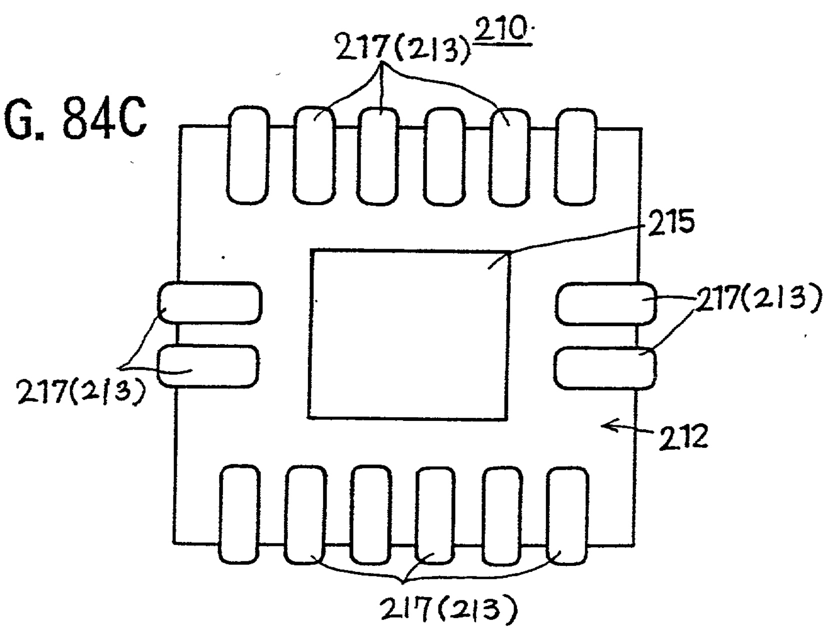


FIG. 85

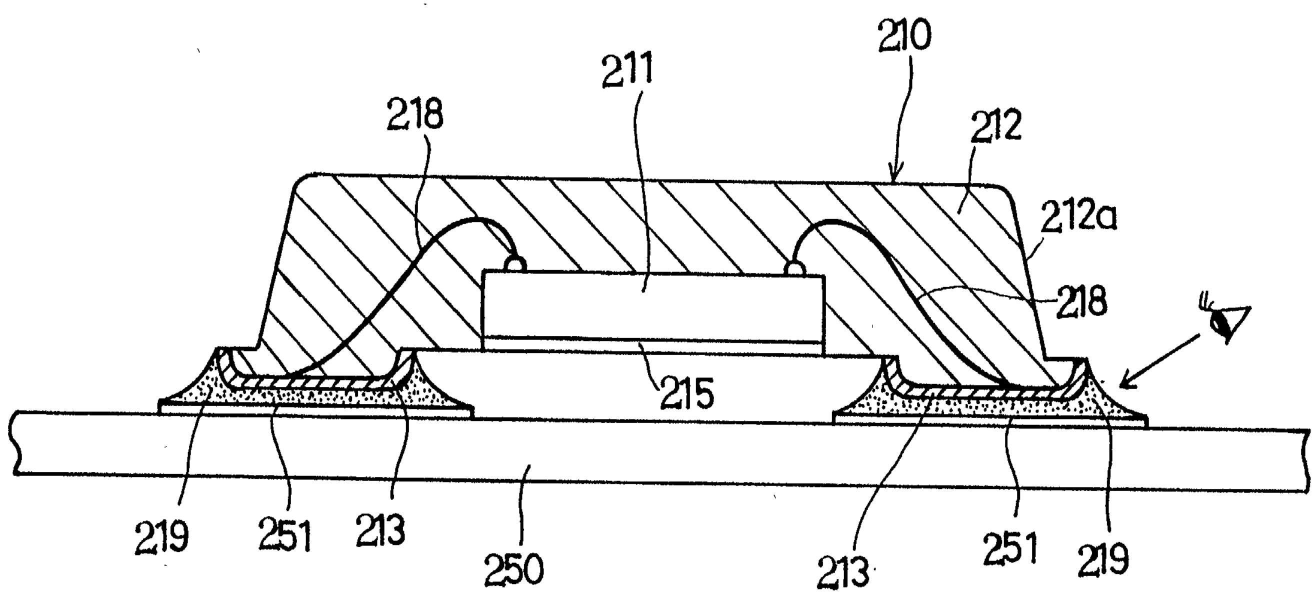


FIG. 86

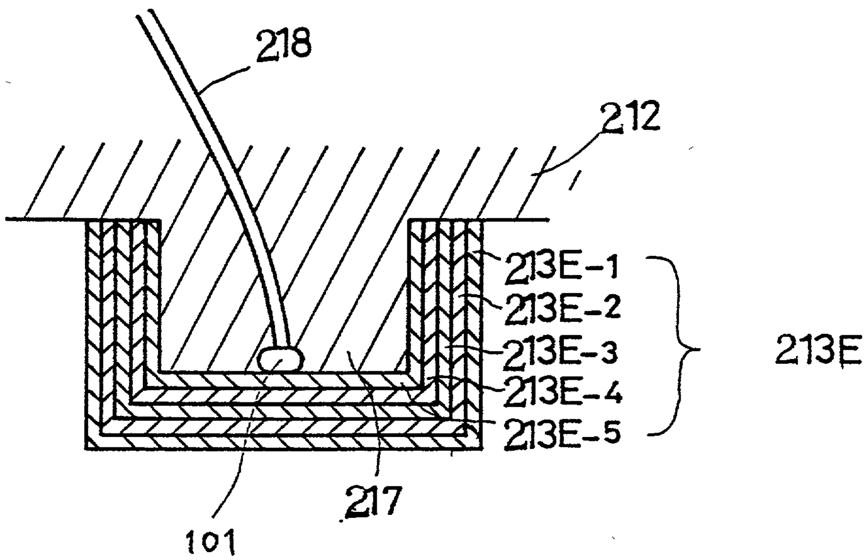


FIG. 87

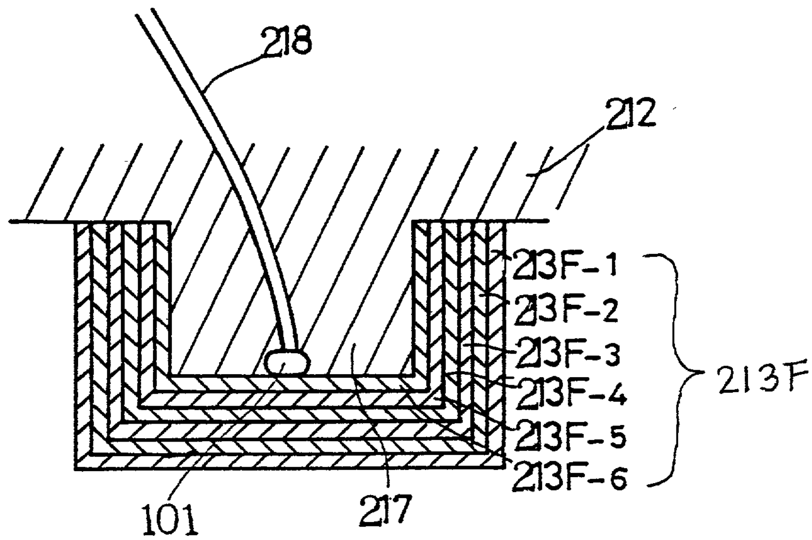

218
212
213F-1
213F-2
213F-3
213F-4
213F-5
213F-6
213F
101
217

FIG. 88

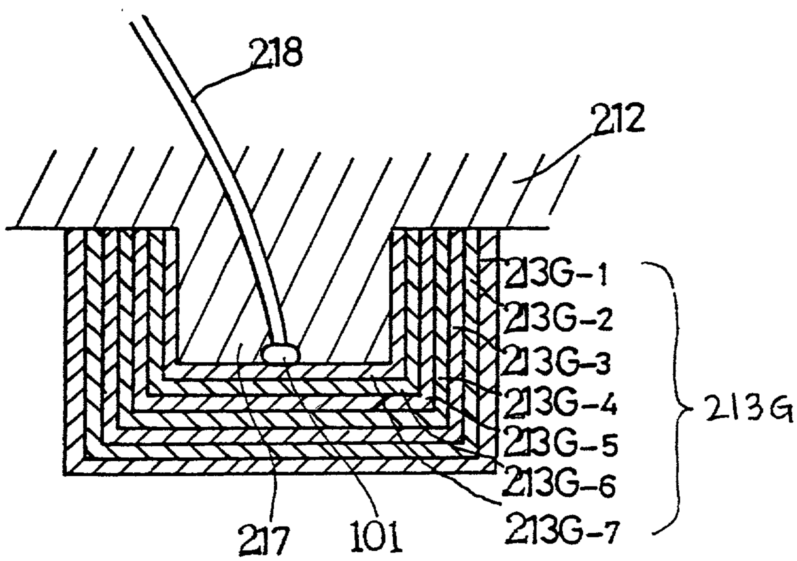

218
212
213G-1
213G-2
213G-3
213G-4
213G-5
213G-6
213G-7
213G
217
101

FIG. 89A

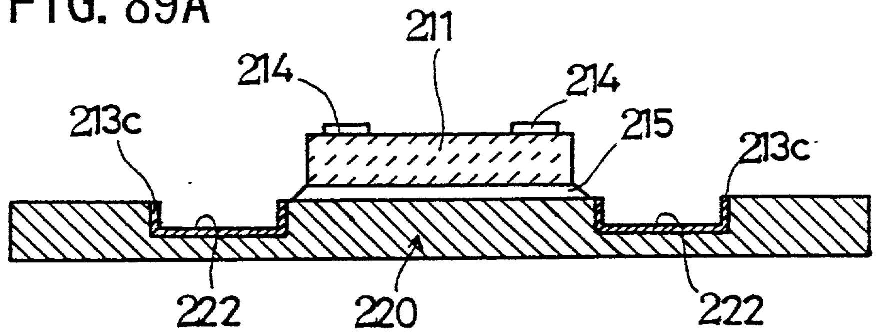


FIG. 89B

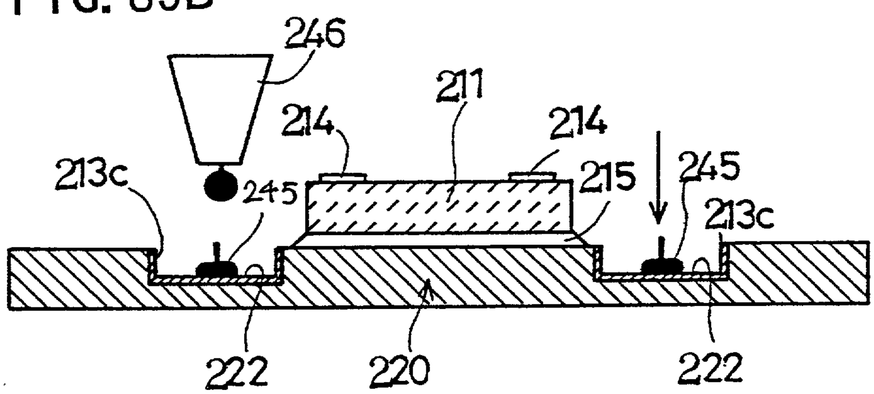


FIG. 89C

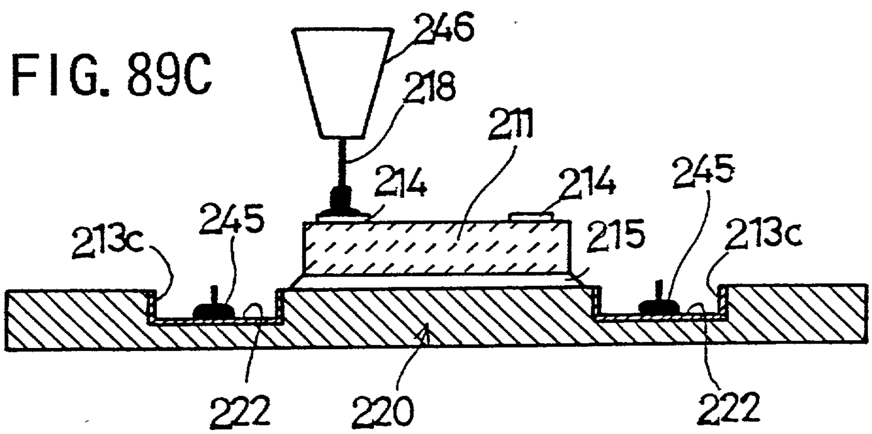


FIG. 89D

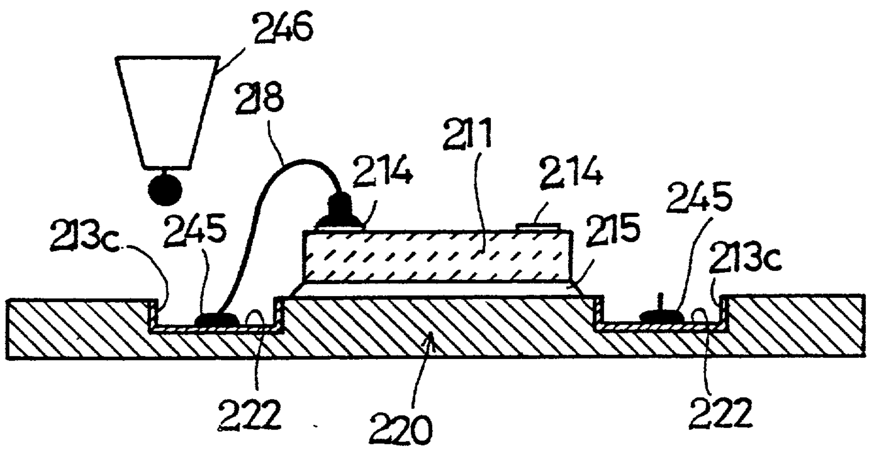


FIG. 89E

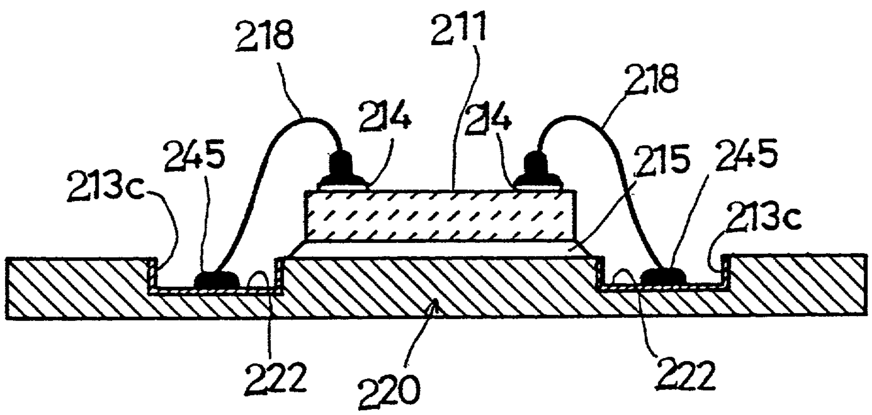


FIG. 90A

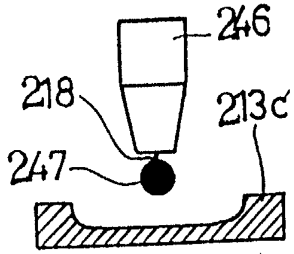


FIG. 90B

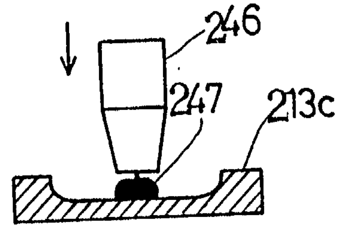


FIG. 90C

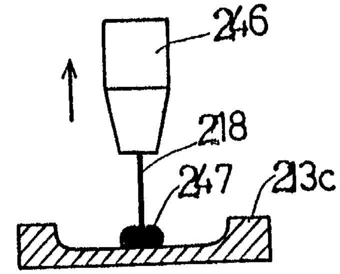


FIG. 90D

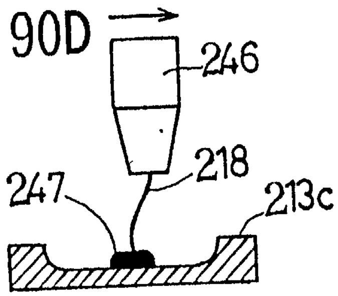


FIG. 90E

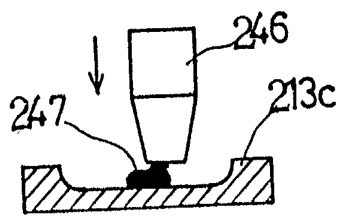


FIG. 90F

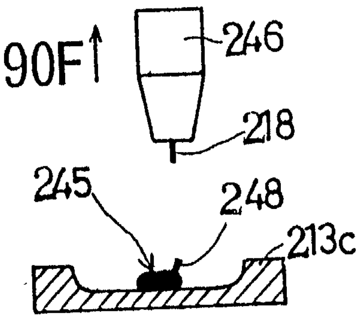


FIG. 90G

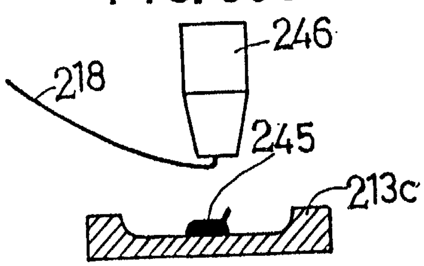


FIG. 90H

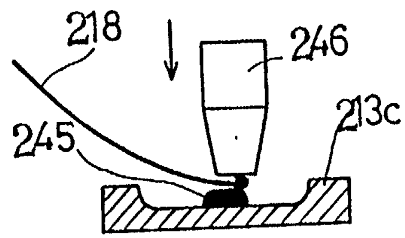


FIG. 90I

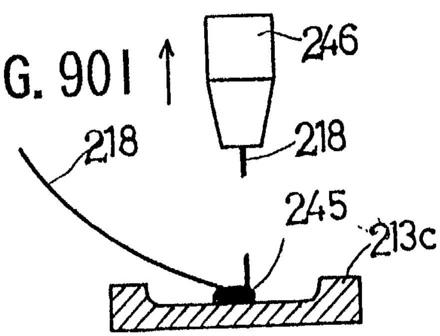
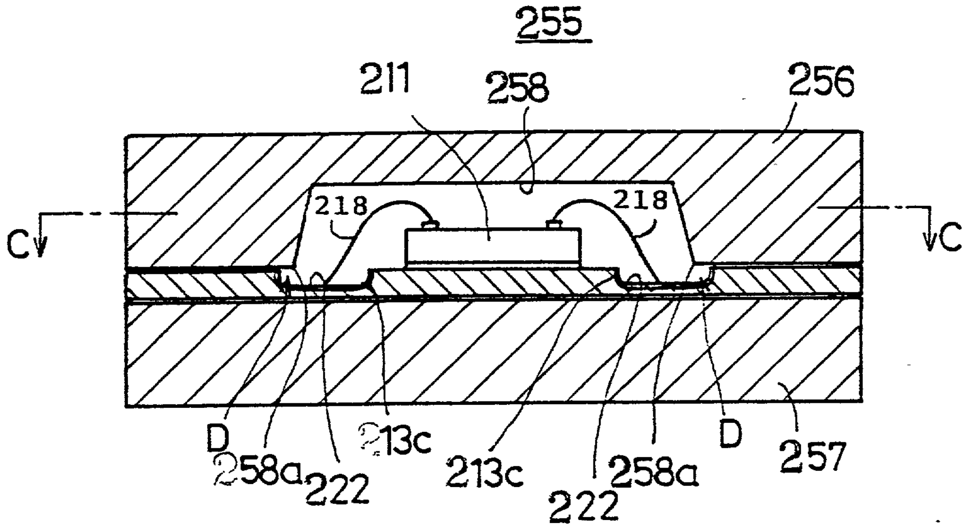
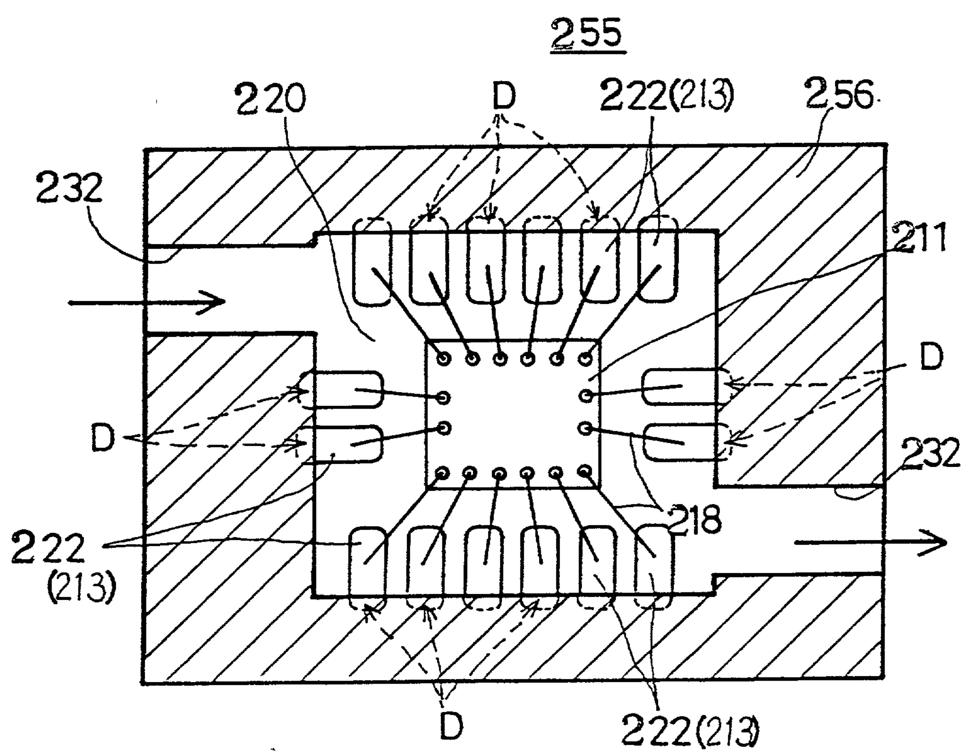


FIG. 91



255
211
258
256
218
218
C
C
D
258a
222
213c
213c
222
258a
D
257

FIG. 92



255
220
D
222(213)
256
232
211
D
D
232
218
222
(213)
D
222(213)

FIG. 93

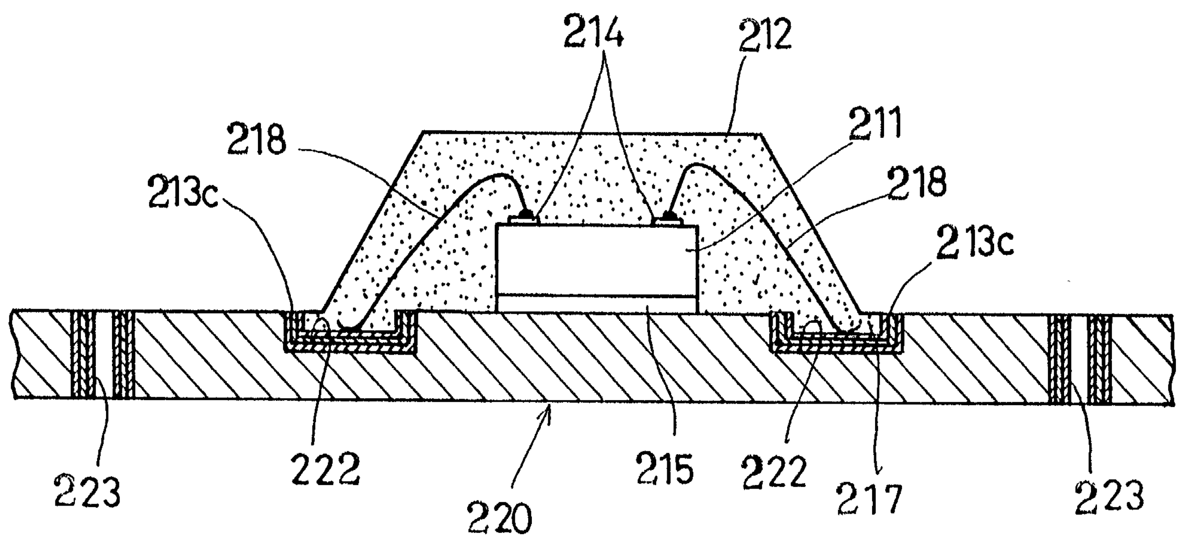


FIG. 94

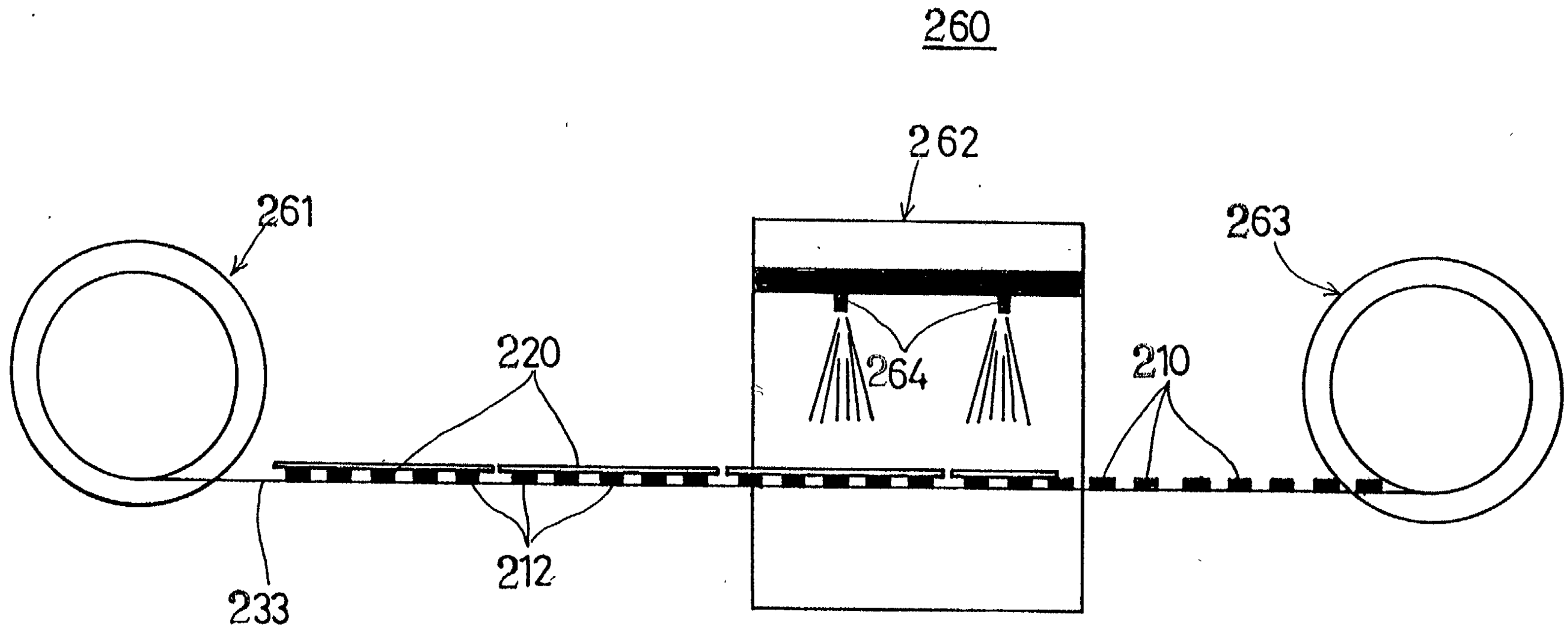


FIG. 95

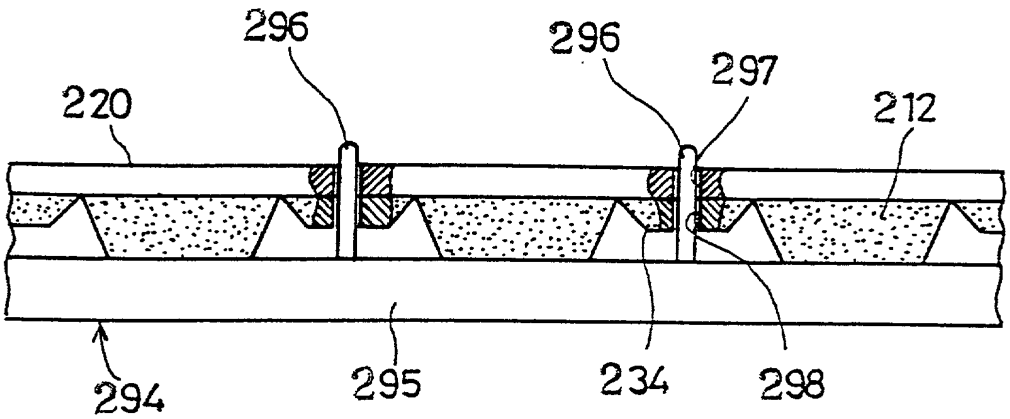


FIG. 96

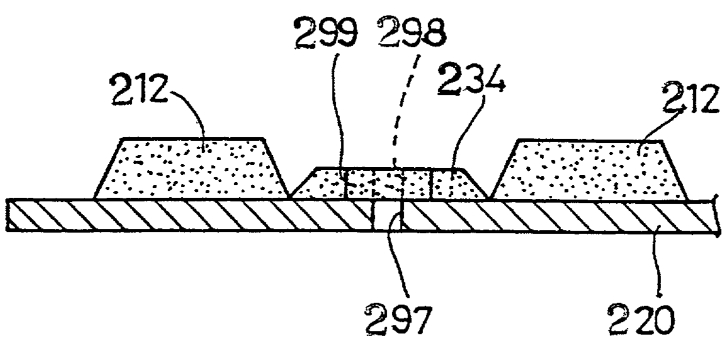


FIG. 97

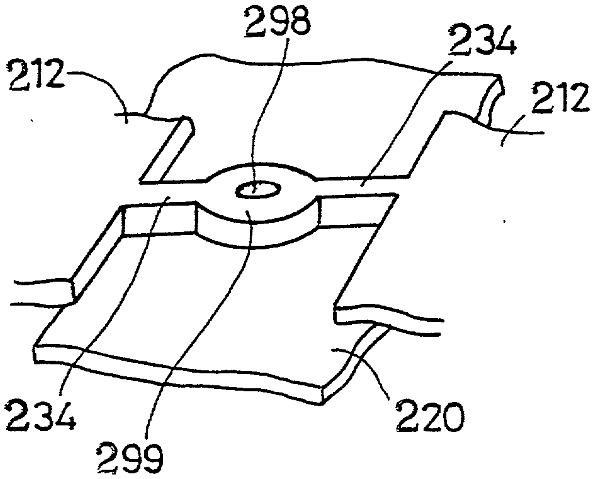


FIG. 98A

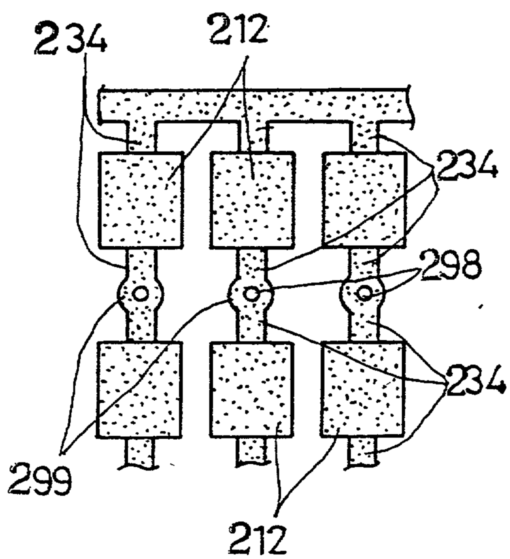


FIG. 98B

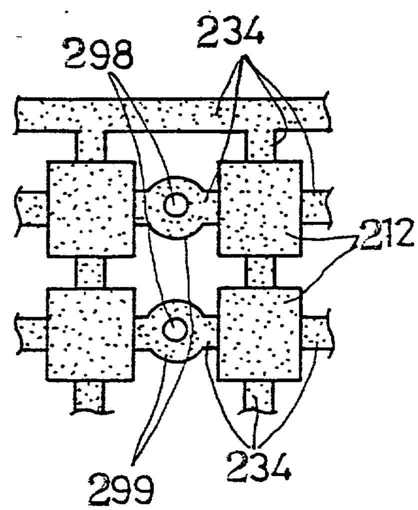


FIG. 99A

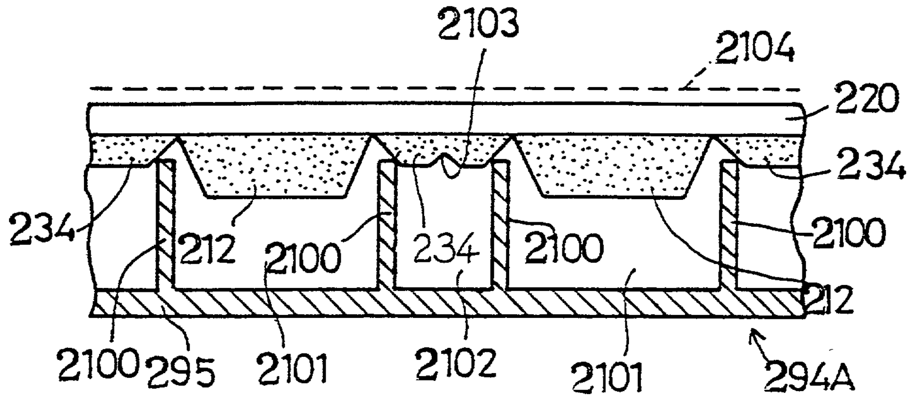


FIG. 99B

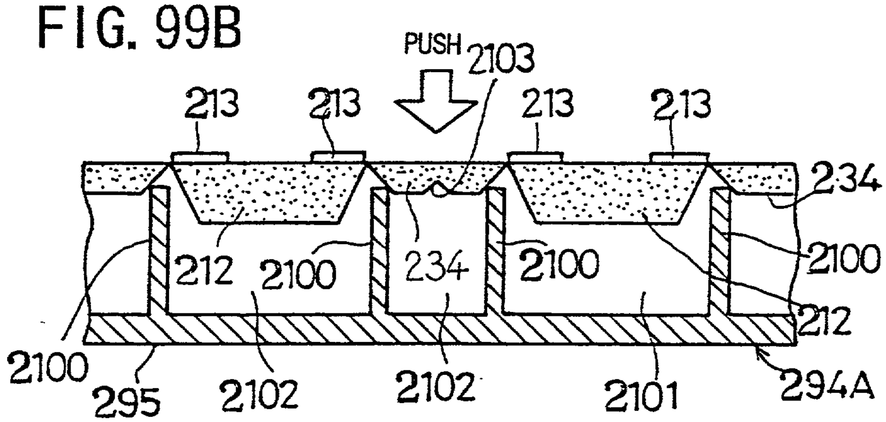


FIG. 99C

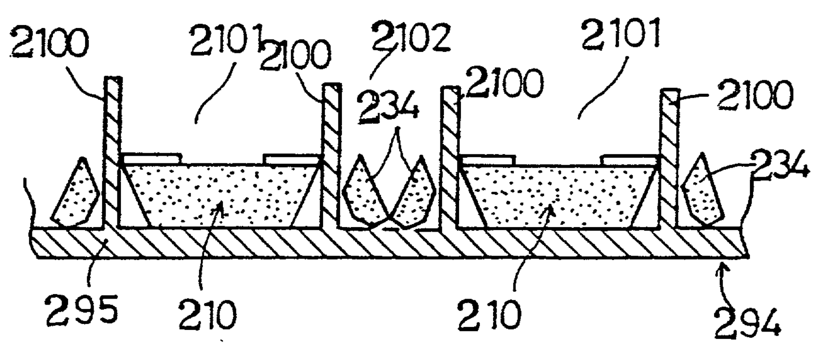


FIG. 100A

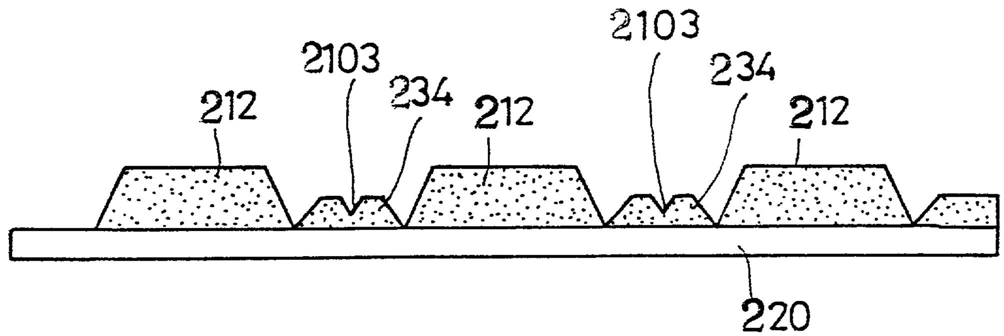


FIG. 100B

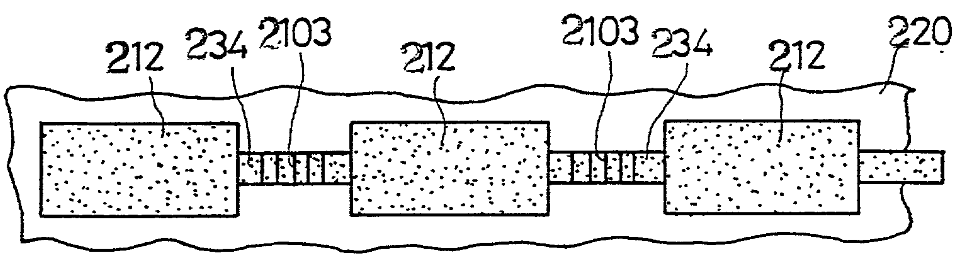


FIG. 101

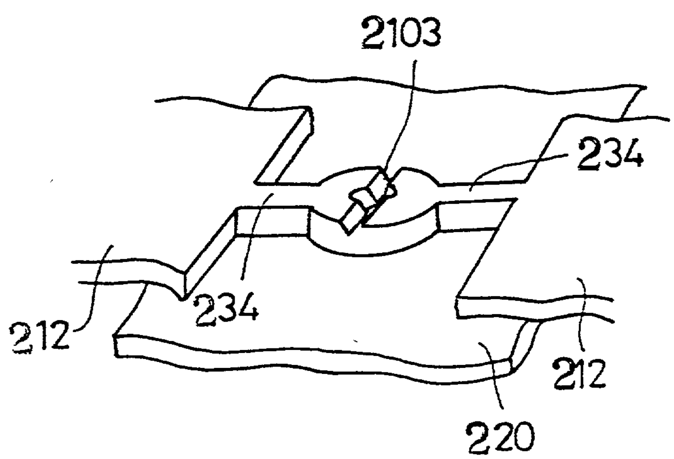


FIG. 102A

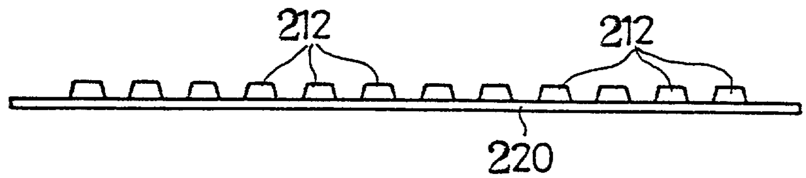


FIG. 102B

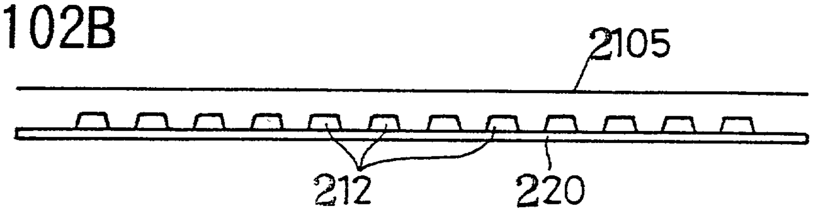


FIG. 102C

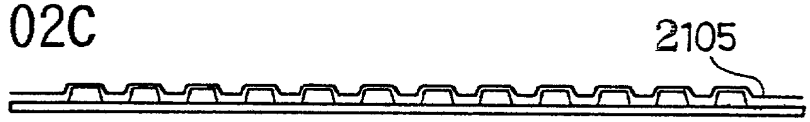


FIG. 102D

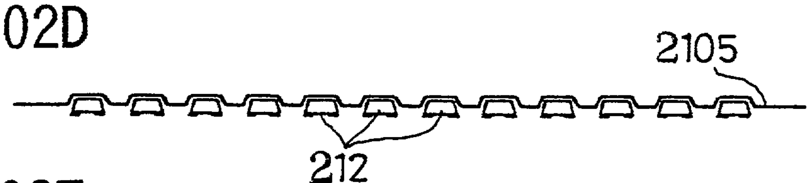


FIG. 102E

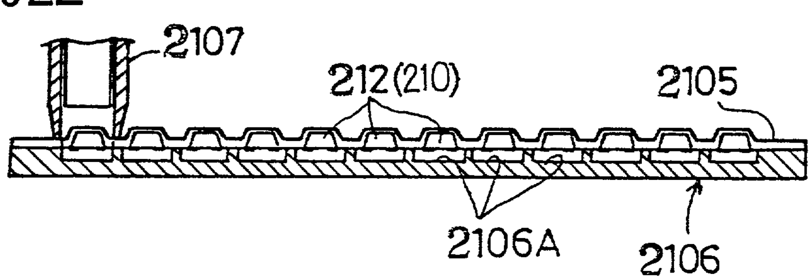


FIG. 103A

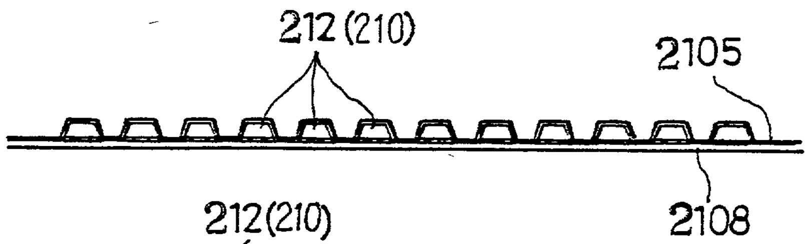


FIG. 103B

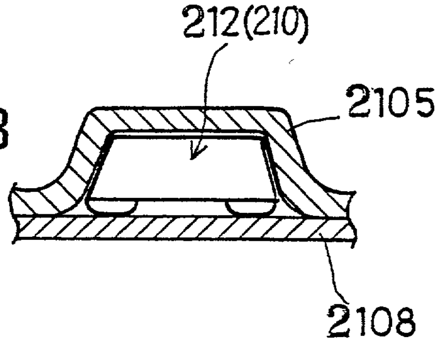


FIG. 104

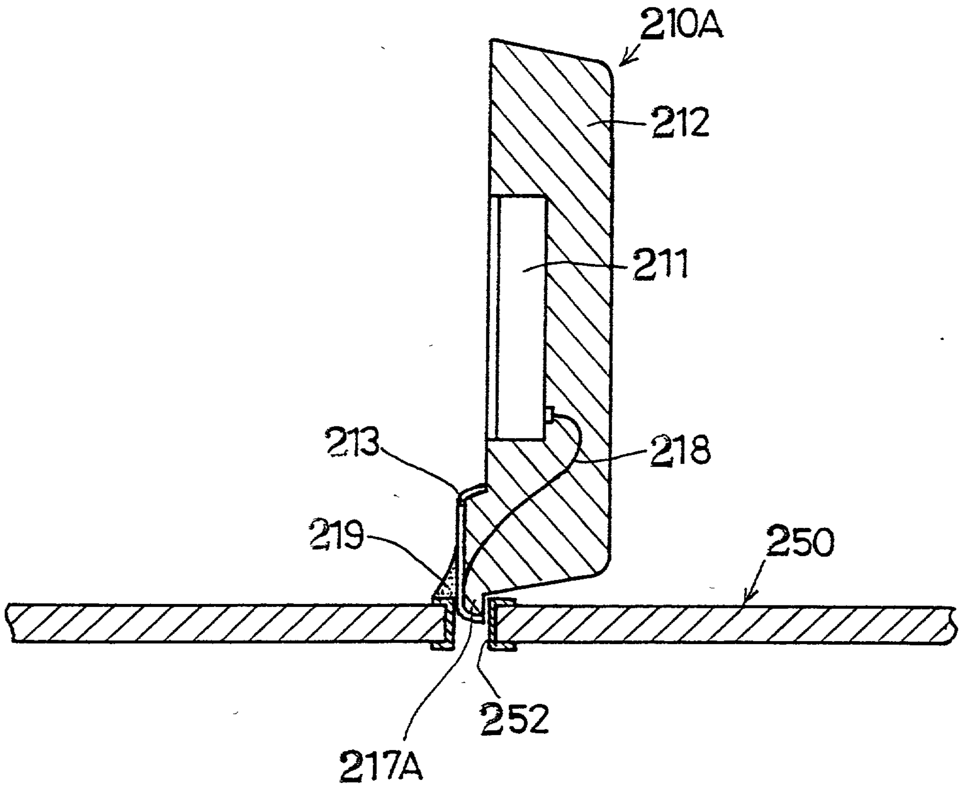


FIG. 105

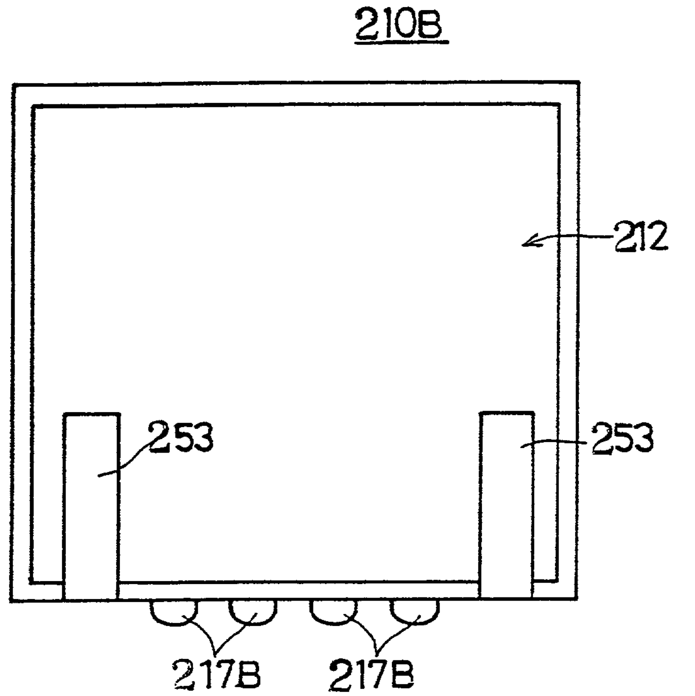


FIG. 106

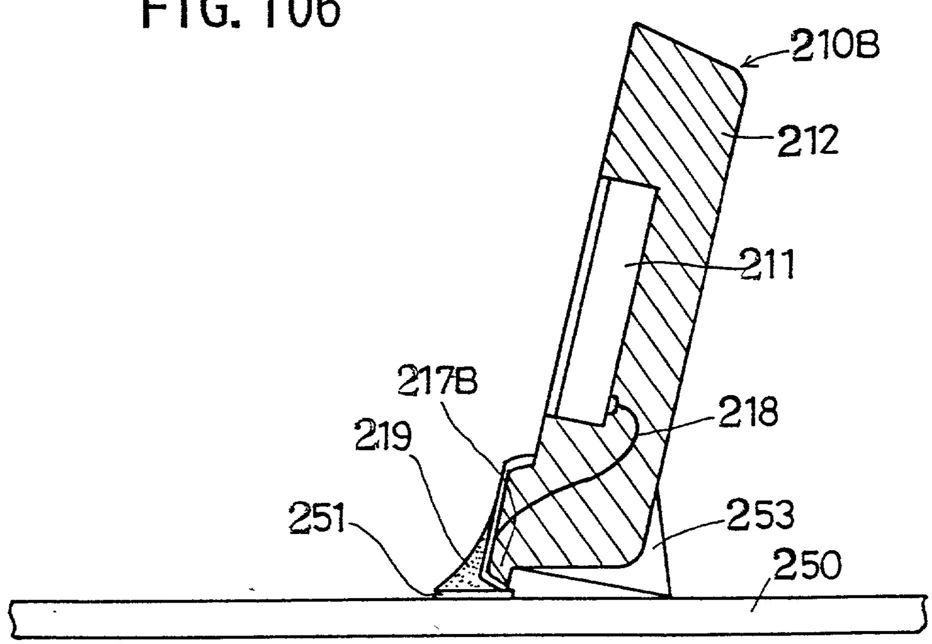


FIG. 107

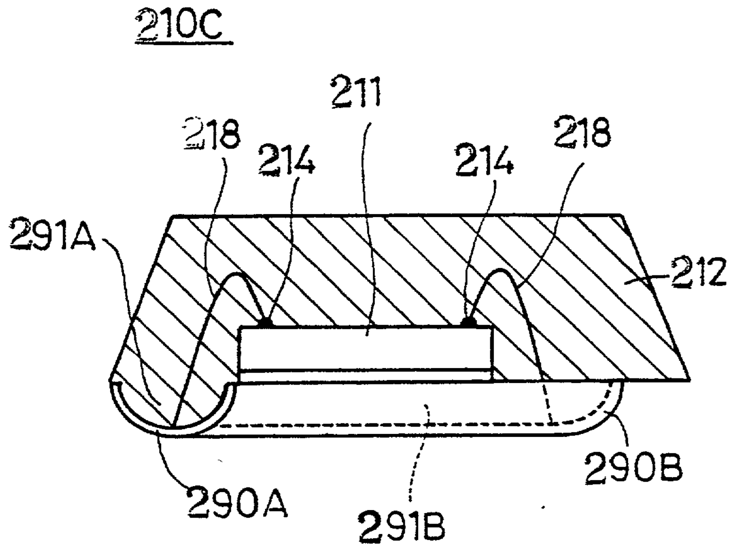


FIG. 108

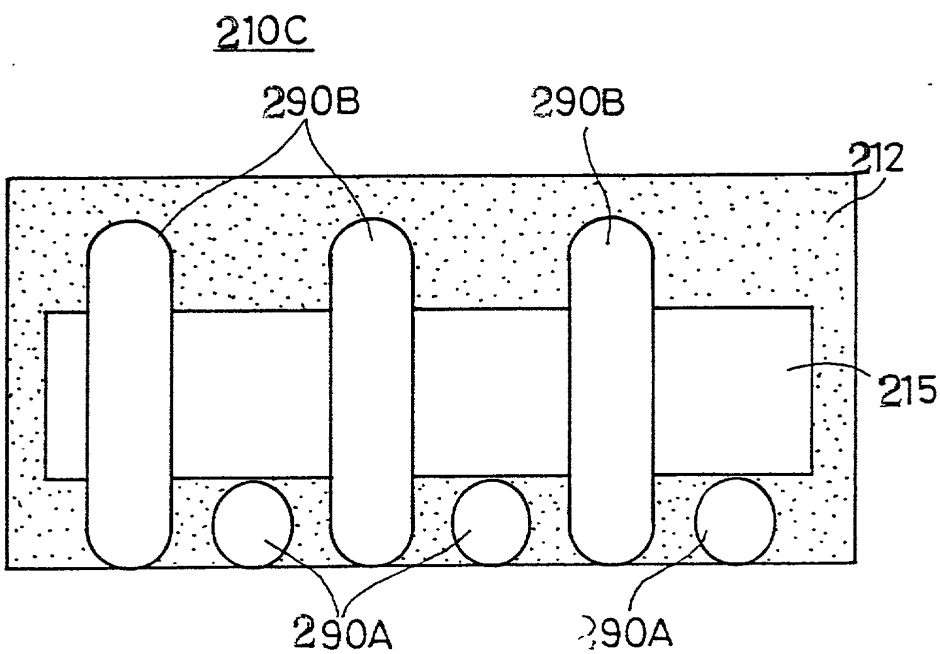


FIG. 109

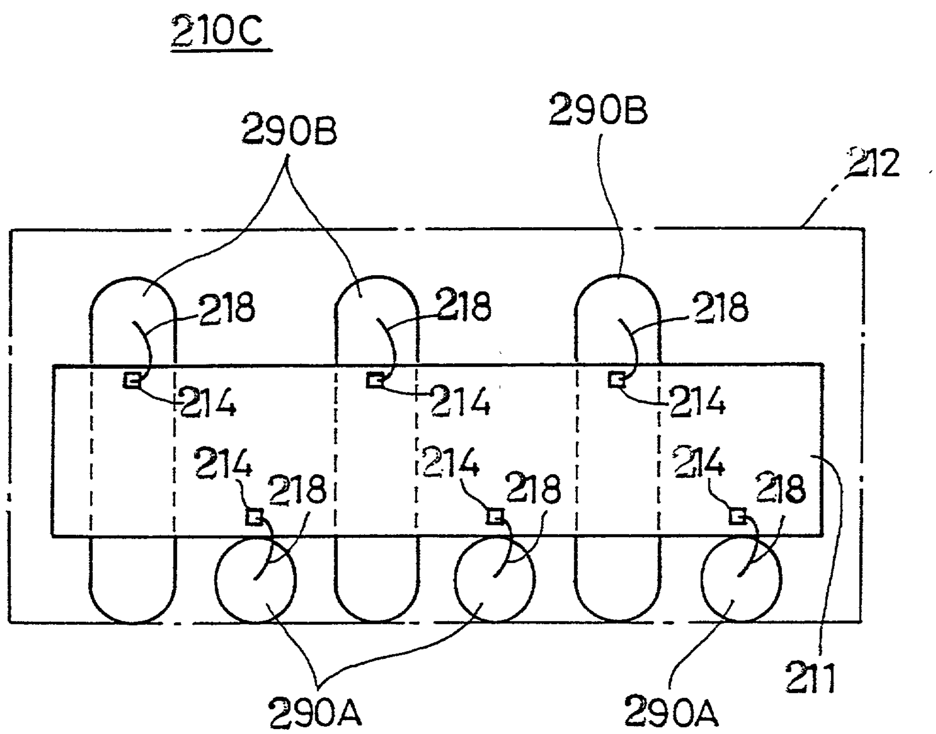

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FIG. 110

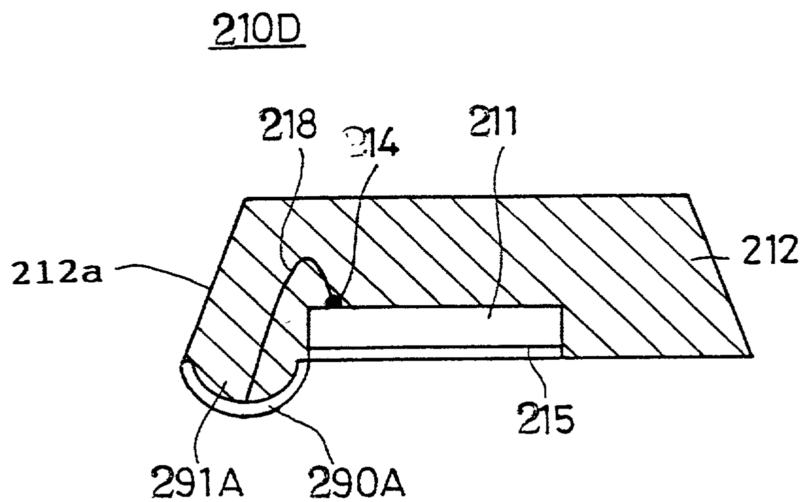


FIG. 111

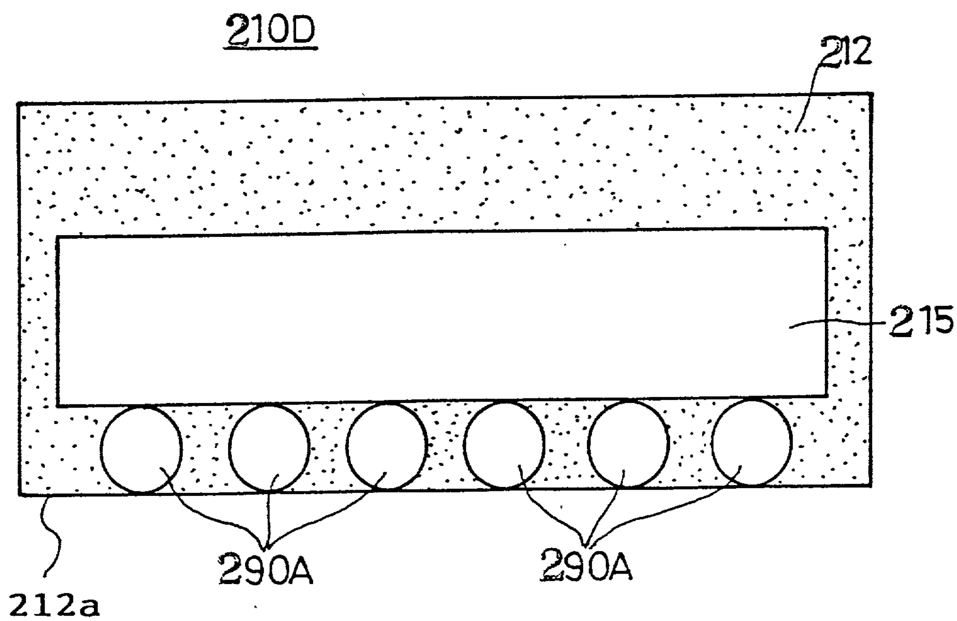
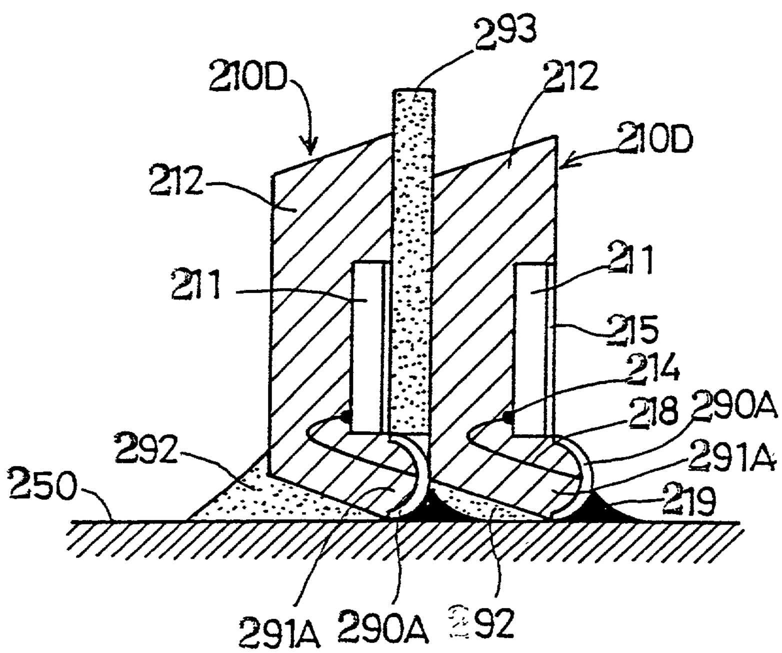


FIG. 112



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292

FIG. 113

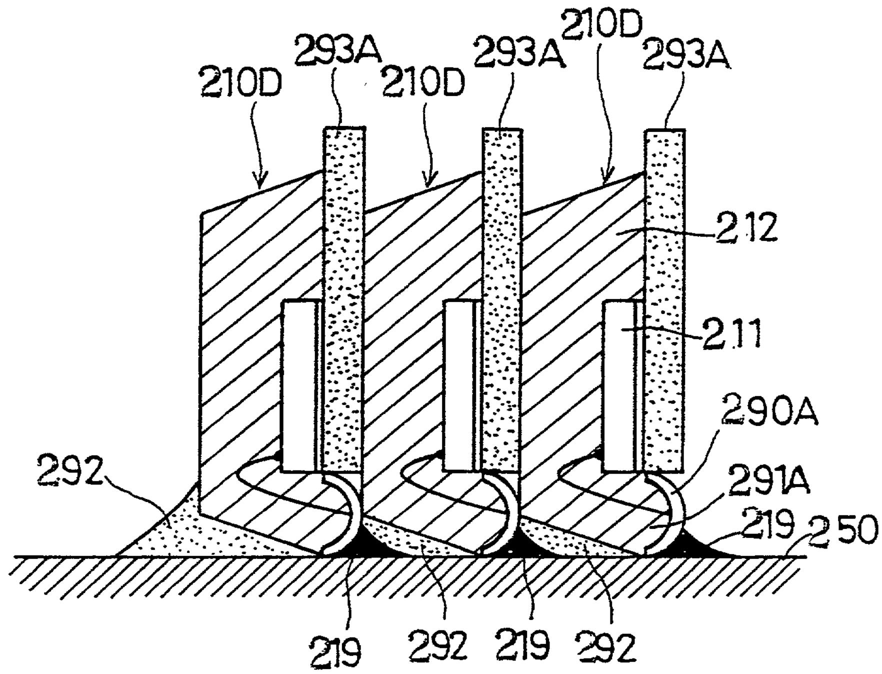


FIG. 114

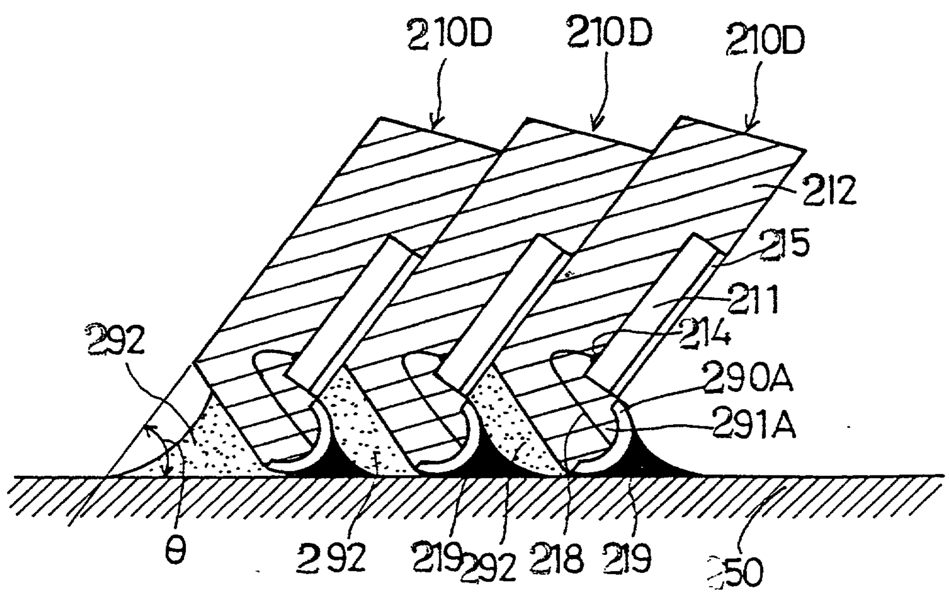


FIG. 115

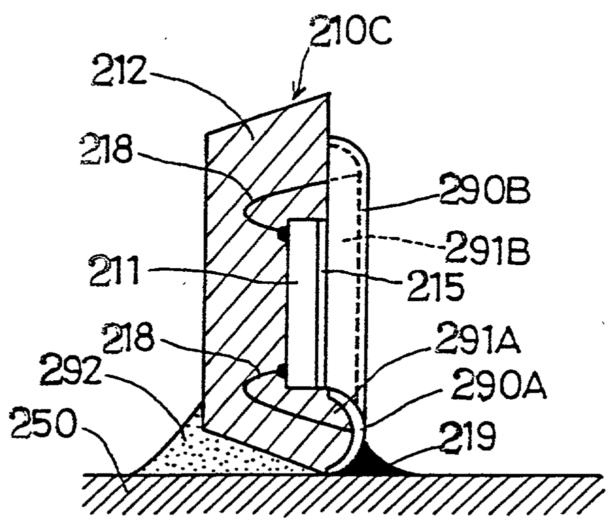


FIG.116

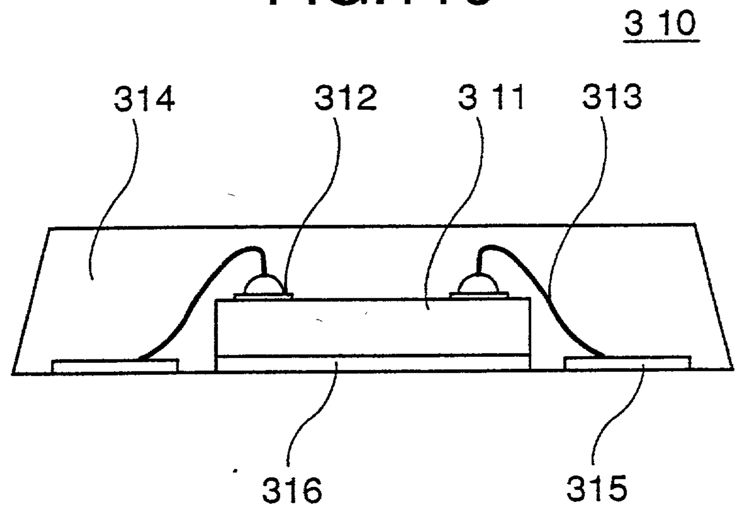


FIG.117

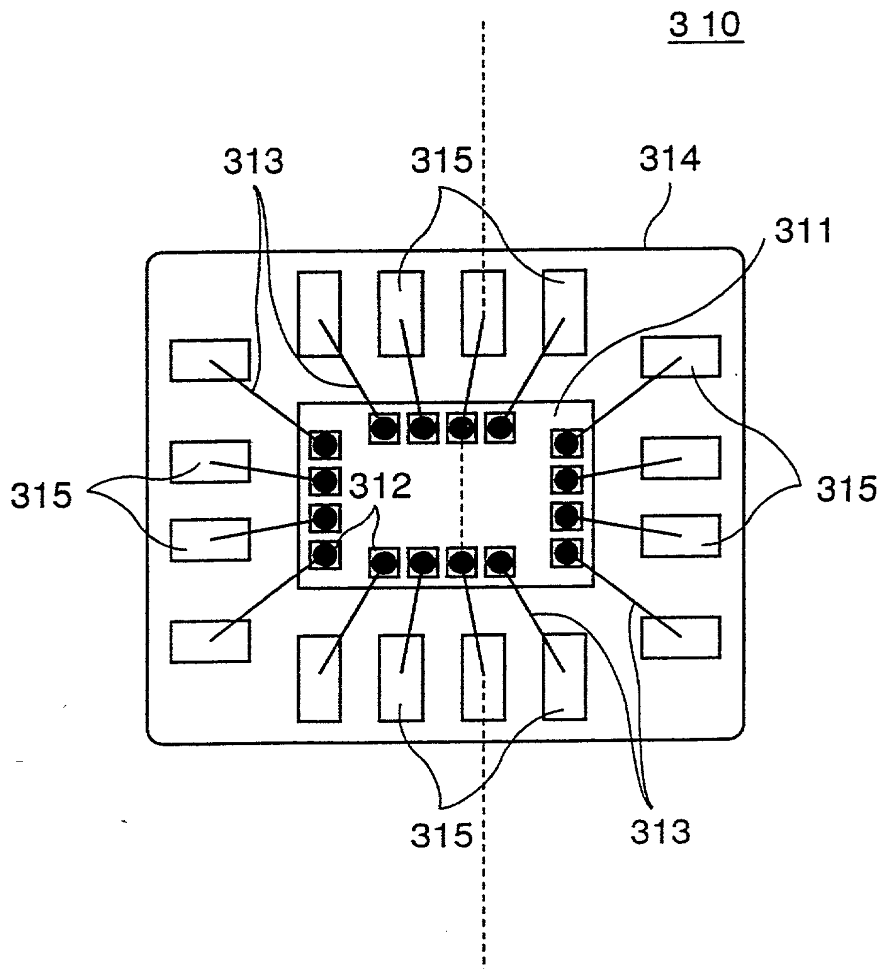


FIG.118

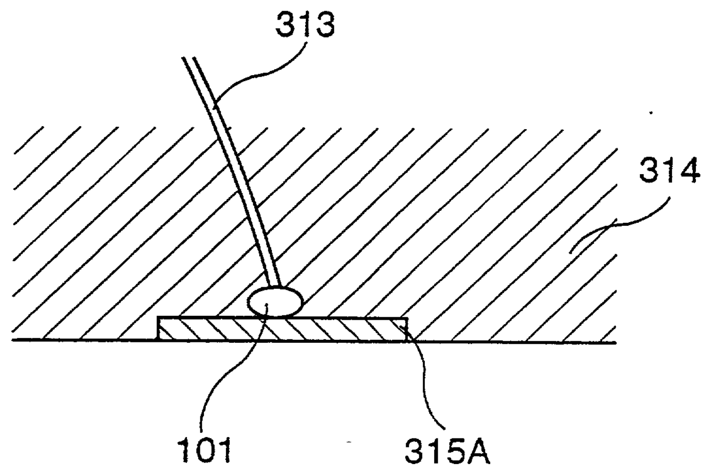


FIG.119

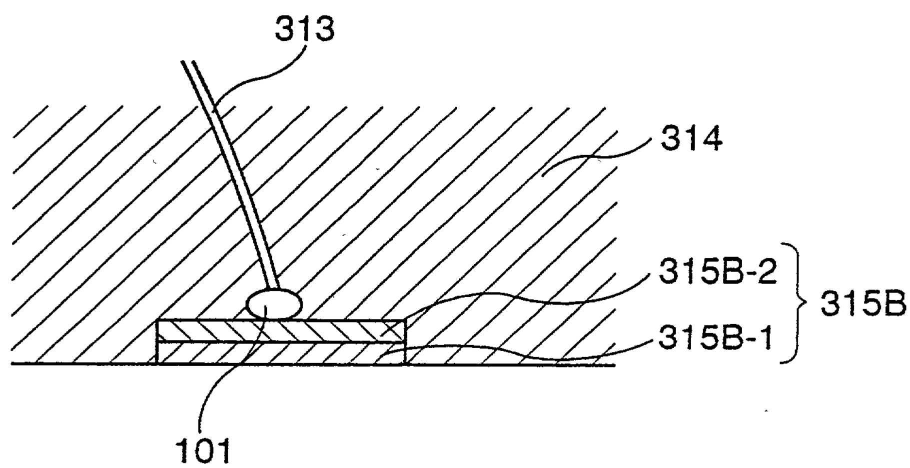


FIG.120

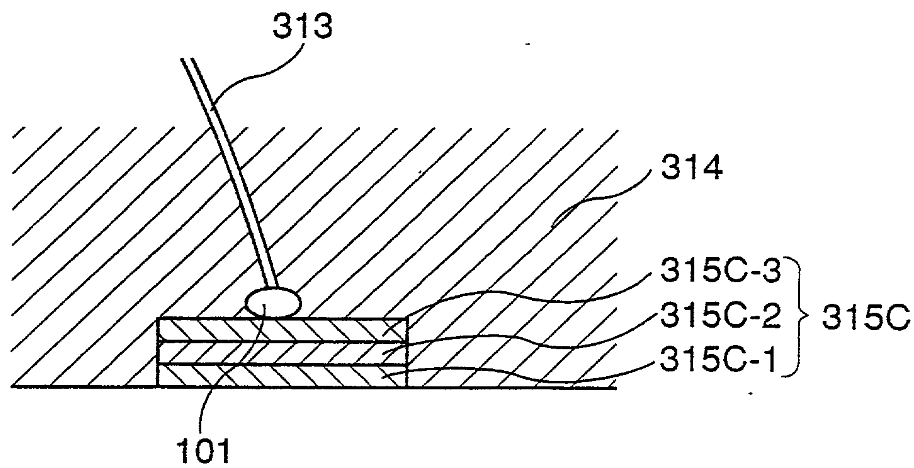


FIG.121

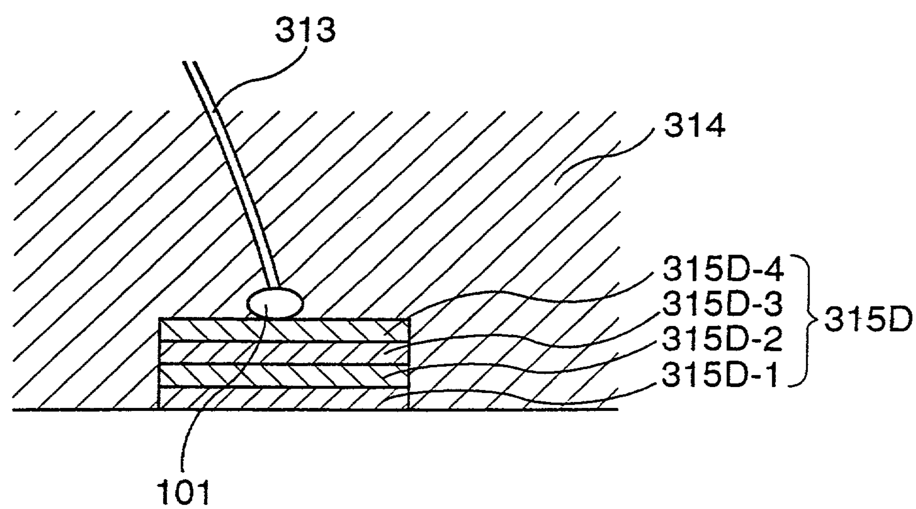


FIG.122

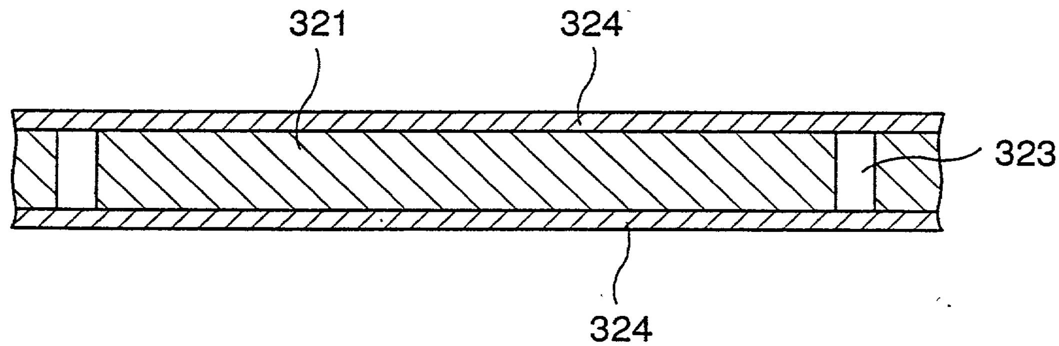


FIG.123

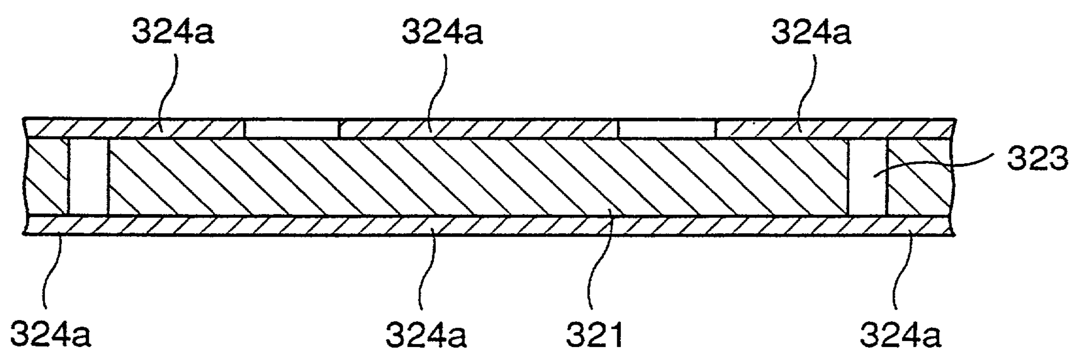


FIG.124

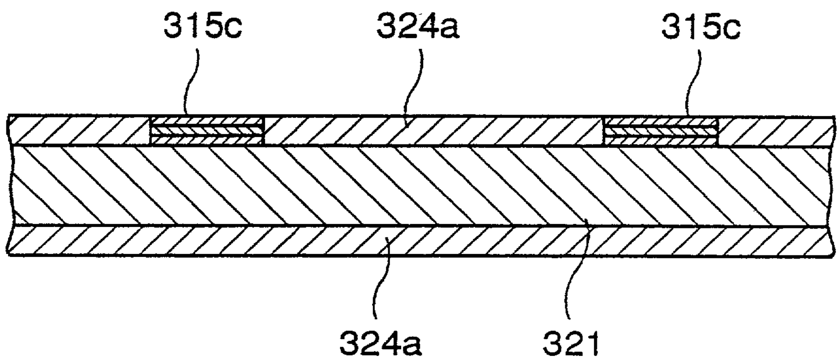


FIG.125

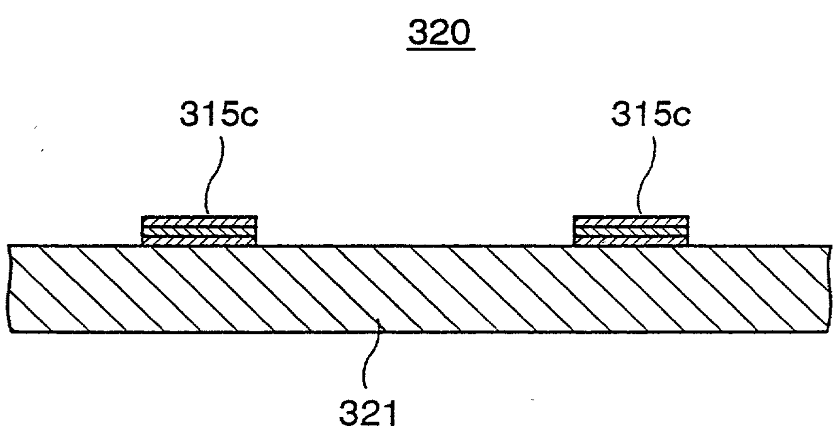


FIG.126

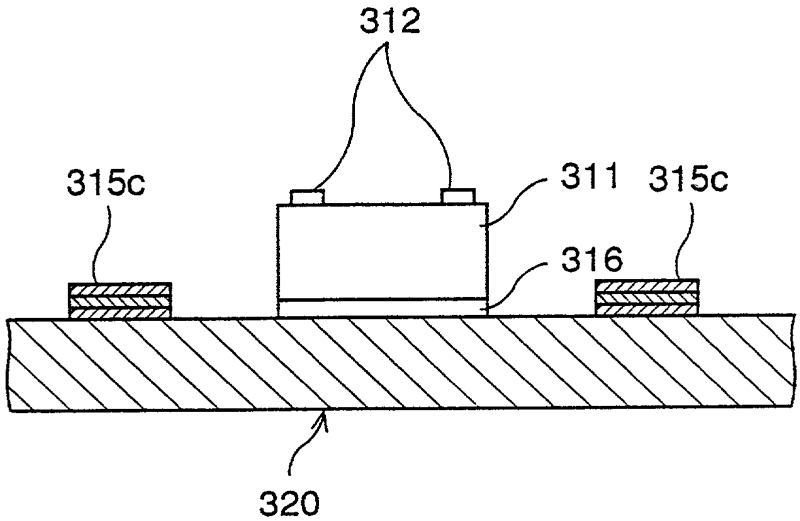


FIG.127

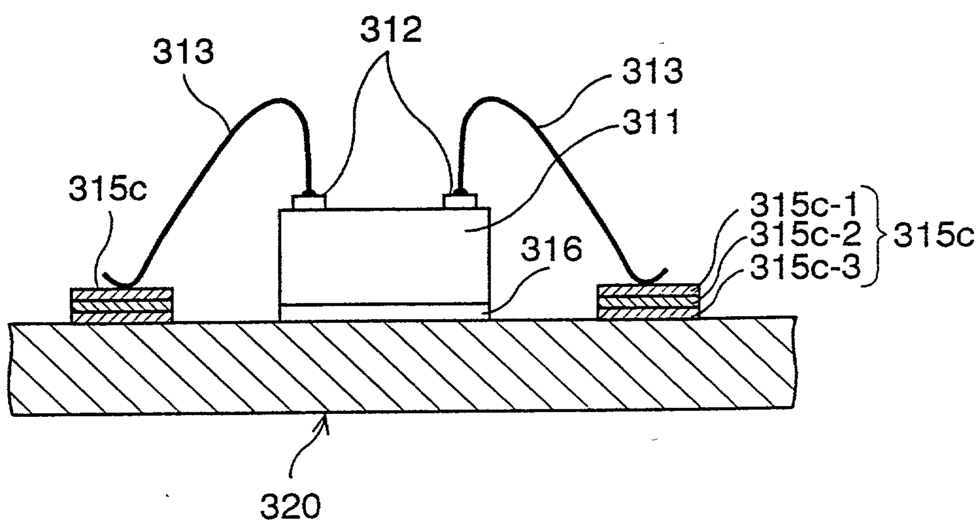


FIG.128

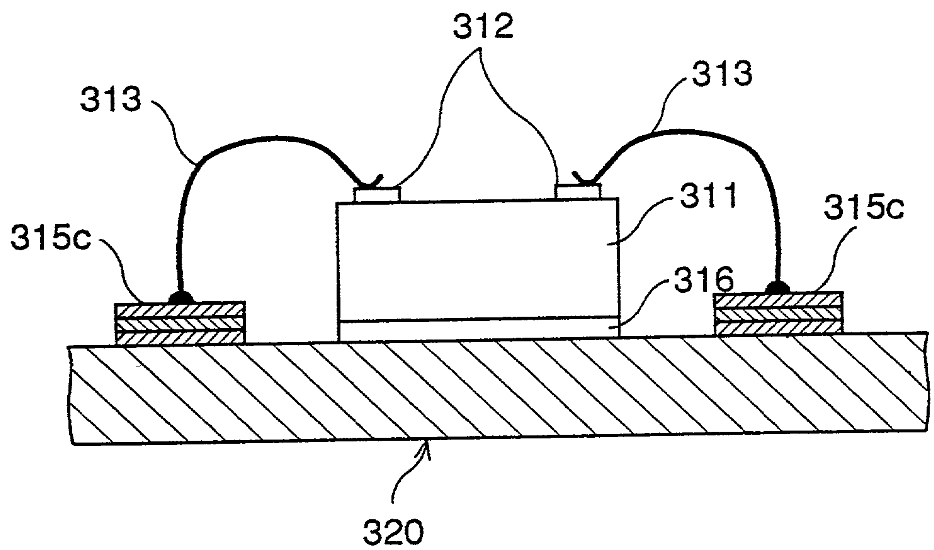


FIG.129

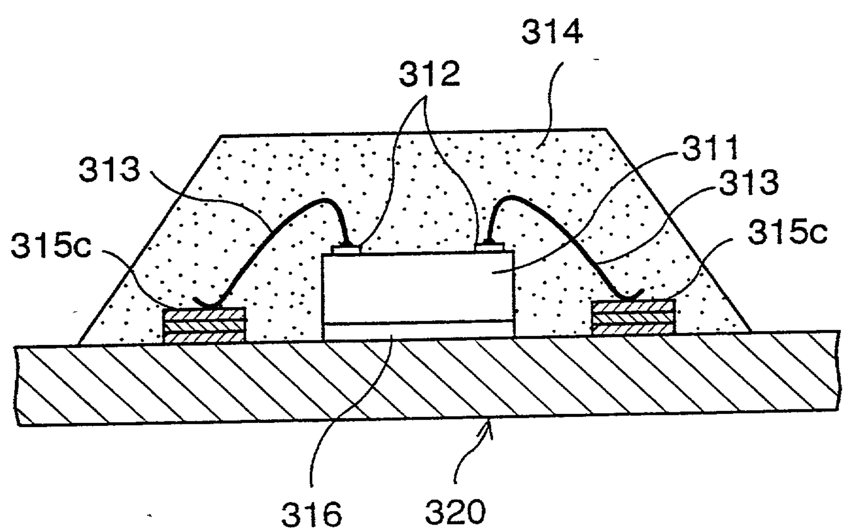
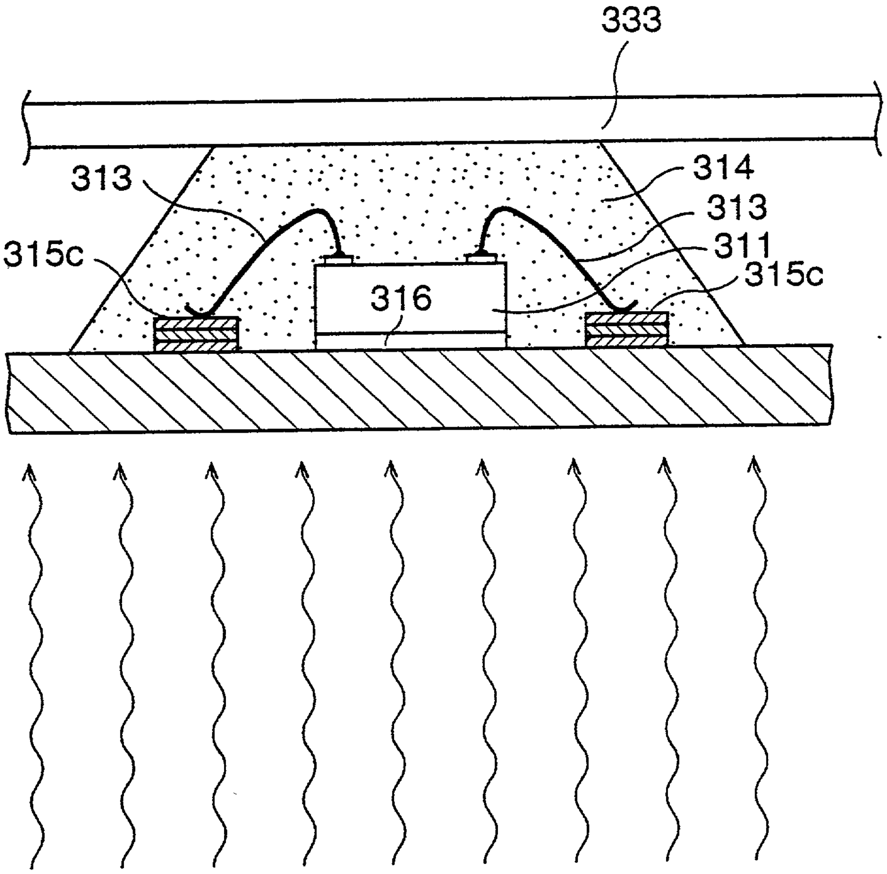


FIG.130



(ETCHING)

FIG.131

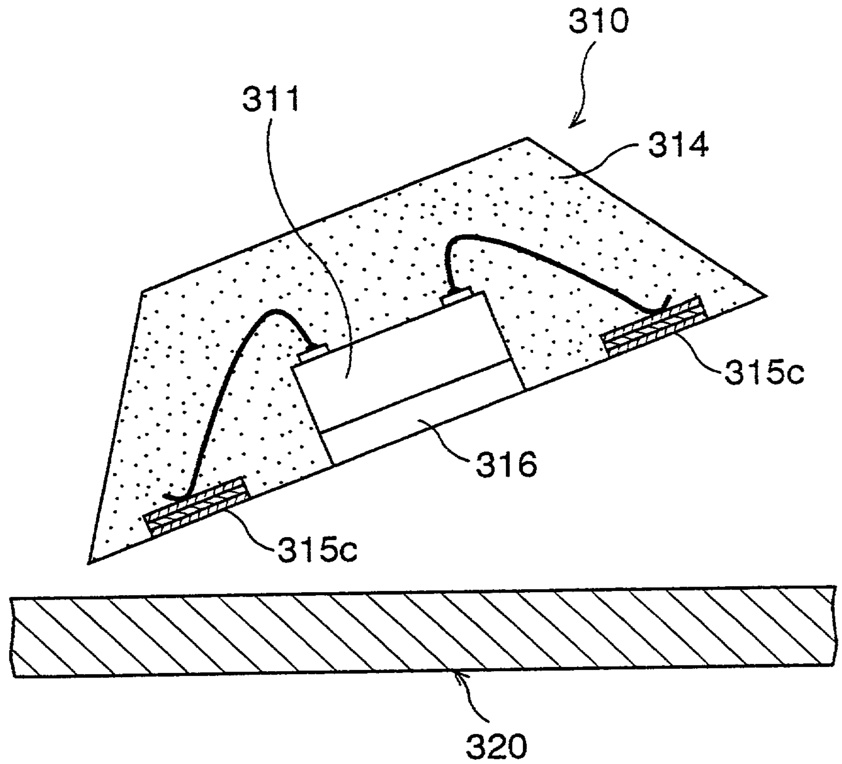


FIG.132A

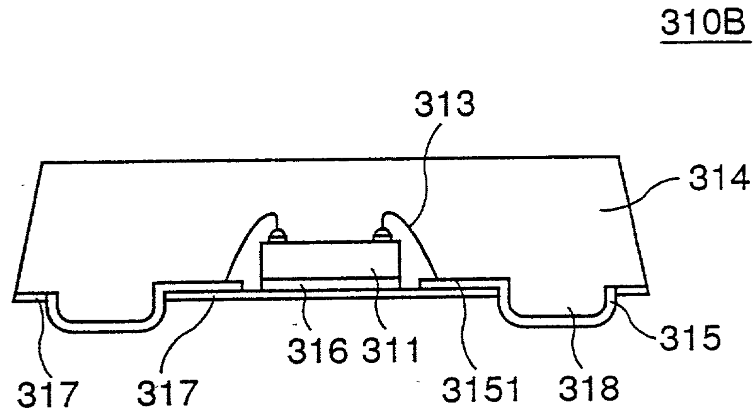


FIG.132B

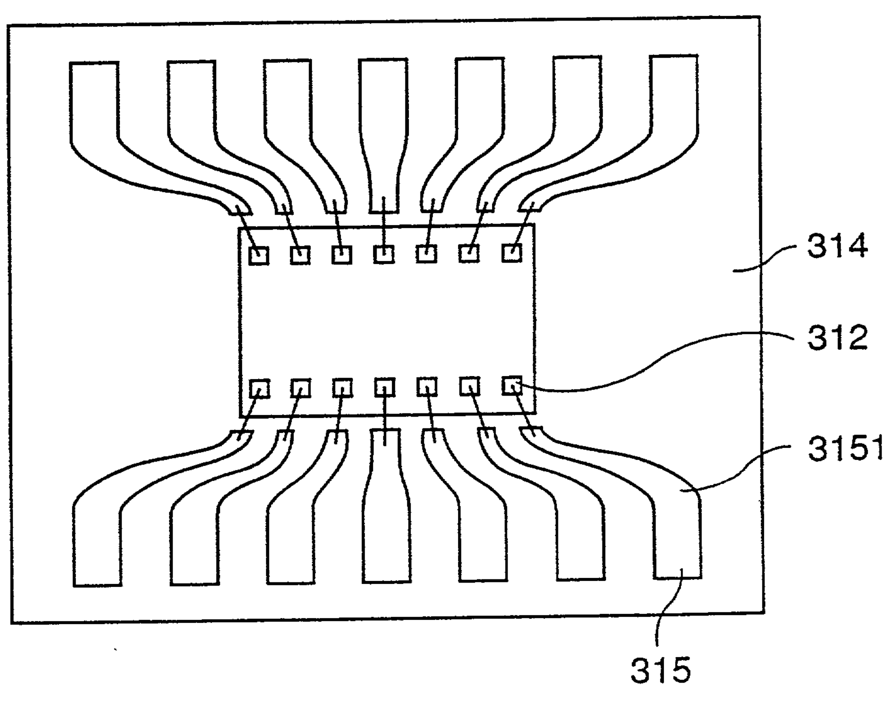


FIG.133

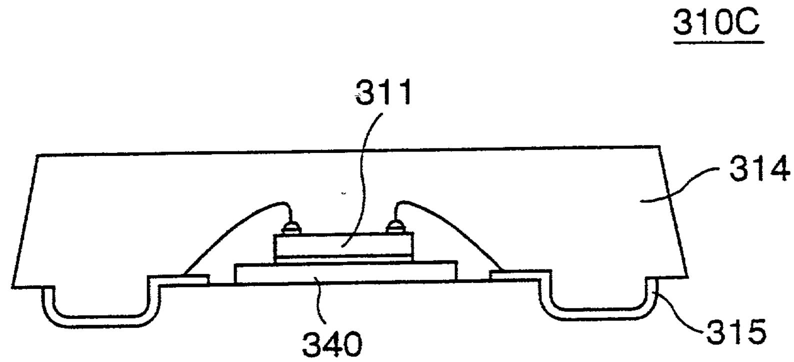


FIG.134

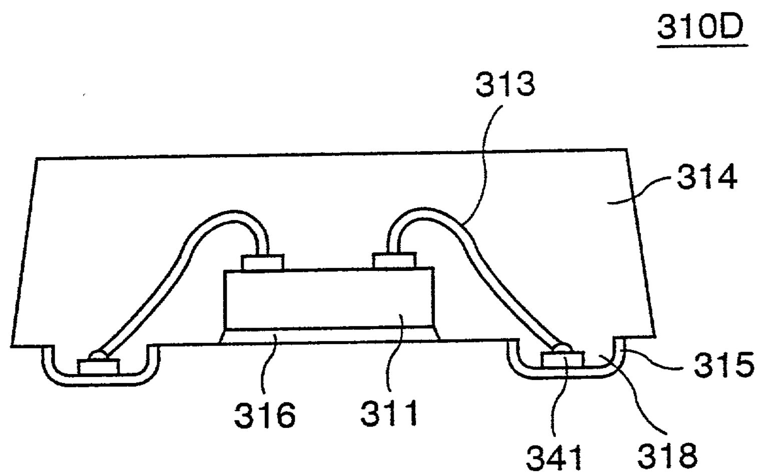


FIG.135

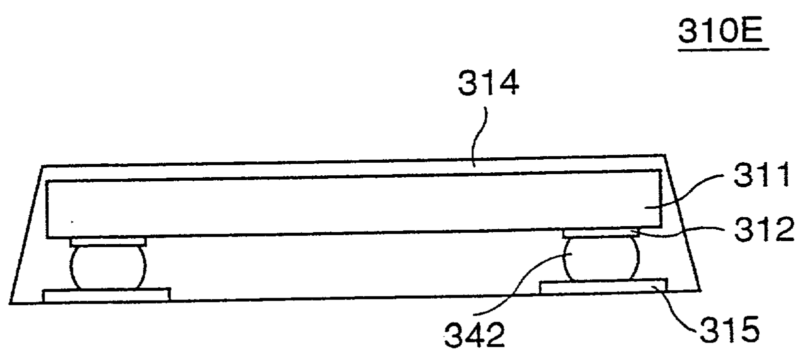


FIG.136A

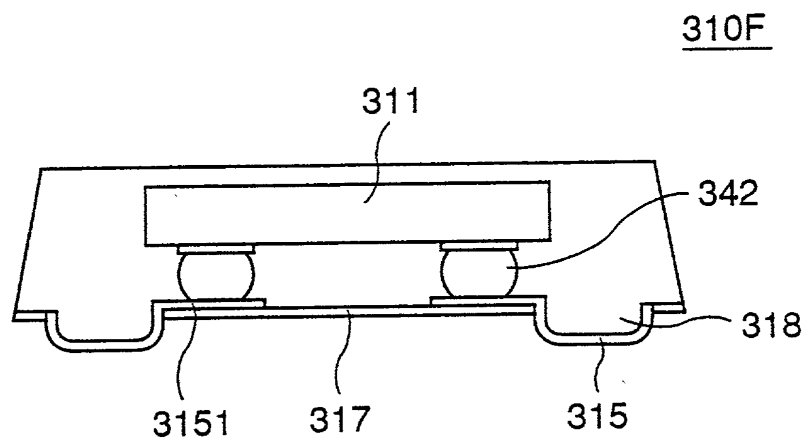


FIG.136B

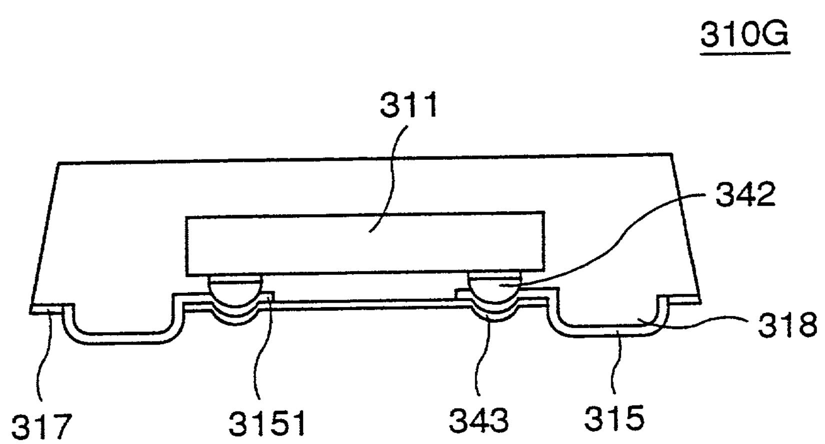


FIG.137

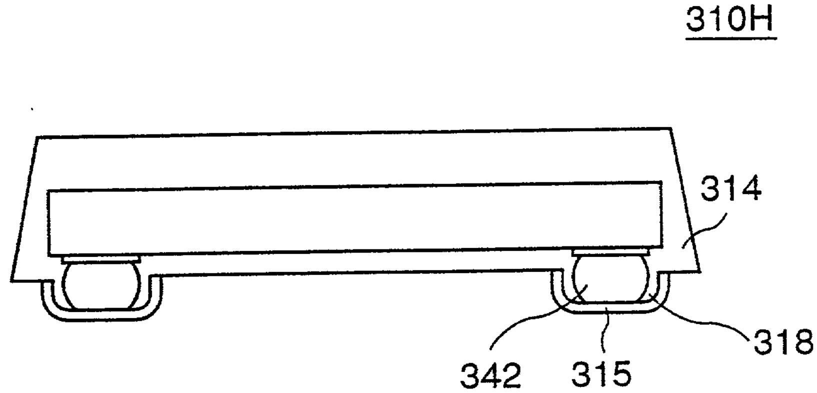


FIG.138

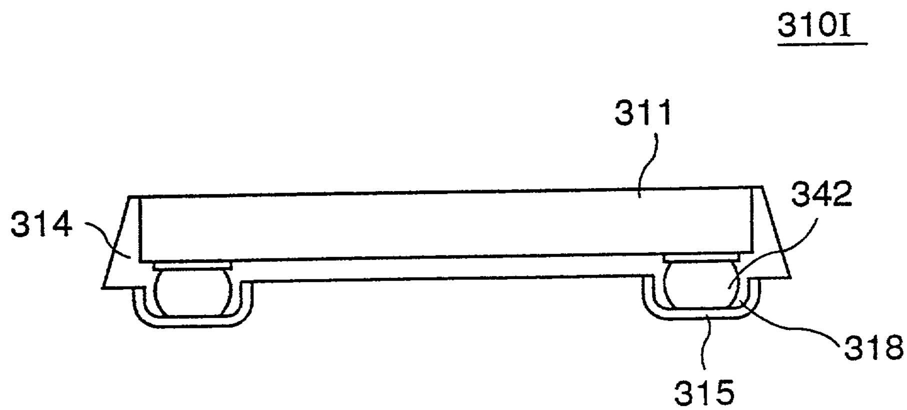


FIG.139A

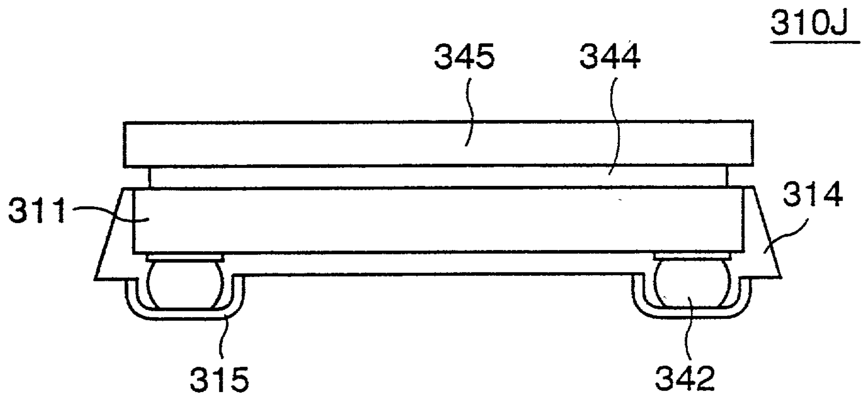


FIG.139B

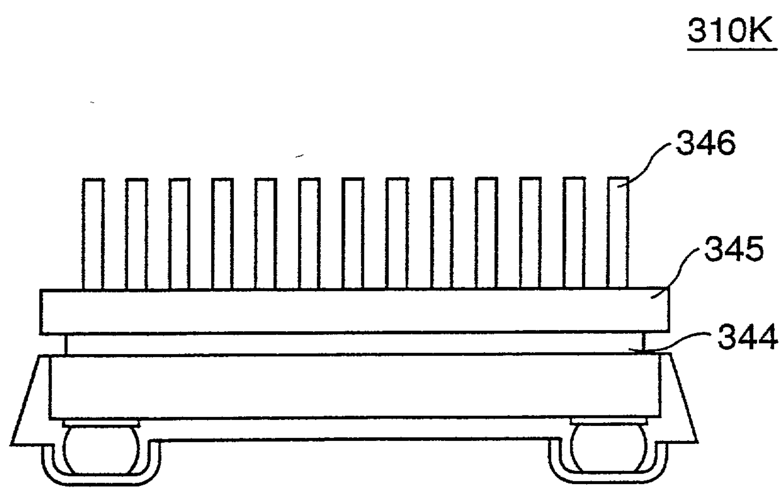


FIG.140

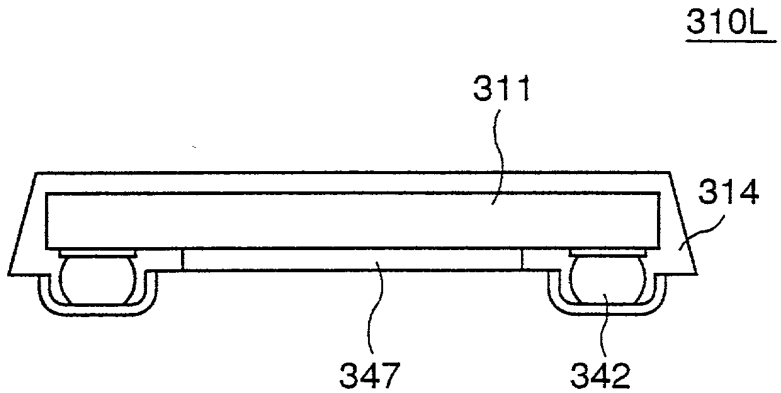


FIG.141A

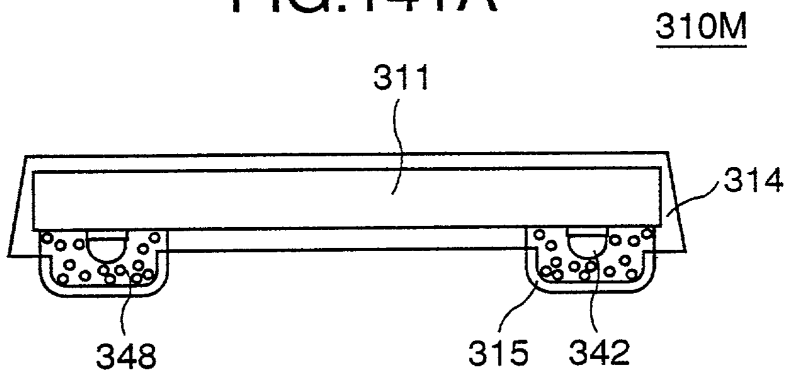


FIG.141B

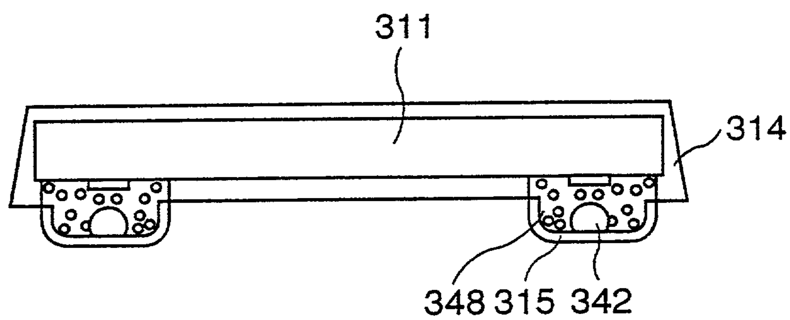
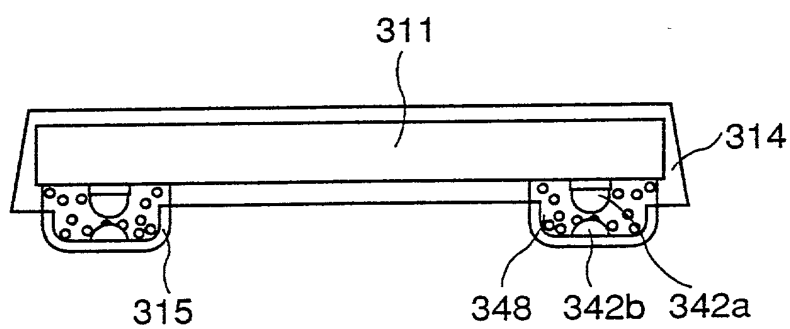


FIG.141C



ARMSTRONG, WES` `MAN, HATTORI, MCLELAND & NAUGHTON
1725 K Str. N.W., Suite 1000, Washington, D.C. 20006

Docket Number (Optional)

DECLARATION FOR U.S. PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled DEVICE HAVING RESIN PACKAGE AND METHOD OF PRODUCING THE SAME

the specification of which is attached hereto unless the following box is checked:

☐ was filed on ______ as United States Application Number or PCT International Application Number ______ and was amended on ______ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.
I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code §119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s) (Number)	(Country)	(Day/Month/Year Filed)	Priority Claimed Yes	No
Pat. Appln. No.7-290135	Japan	8/November/1995	XX	
No.8-183838	Japan	12/July/1996	XX	

XX See attached list for additional prior foreign applications.

I hereby claim the benefit under Title 35, United States Code §119(e) of any United States provisional application(s) listed below.

(Application Number) (Filing Date)

(Application Number) (Filing Date)

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

(Application Number) (Filing Date) (Status -- patented, pending, abandoned)

(Application Number) (Filing Date) (Status -- patented, pending, abandoned)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

James E. Armstrong, III, Reg. No. 18,366; William F. Westerman, Reg. No. 29,988; Ken-Ichi Hattori, Reg. No. 32,861; John R. Pegan, Reg. No. 18,069; William G. Kratz, Jr., Reg. No. 22,631; Le-Nhung McLeland, Reg. No. 31,541; James P. Welch, Reg. No. 17,379; Ronald F. Naughton, Reg. No. 24,616; Albert Tockman, Reg. No. 19,722; Mel R. Quintos, Reg. No. 31,898; Michael J. Foycik, Jr., Reg. No. 30,928; Donald W. Hanson, Reg. No. 27,133; Stephen G. Adrian, Reg. No. 32,878; William L. Brooks, Reg. No. 34,129; Stephen B. Parker, Reg. No. 36,631; John F. Carney, Reg. No. 20,276; Edward F.Welsh, Reg. No. 22,455; Patrick D. Muir, Reg. No. 37,403; Gay A. Spahn, Reg. No. 34,978; and Theresa M. Stevens-Smith, Reg. No. 36,281.

Address all telephone calls to Armstrong, Westerman, Hattori, McLeland & Naughton at telephone number 202-659-2930.

Address all correspondence to: **Armstrong, Westerman, Hattori, McLeland & Naughton**
1725 K Street, N.W., Suite 1000
Washington, DC 20006

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Prior Foreign Application(s) (Patent)

			Priority Claimed	
No. 7-322803	Japan	12/December/1995	☒	☐
(Number)	(Country)	Day/Month/Year Filed)	Yes	No
No.8-250707	Japan	20/September/1996	☒	☐
(Number)	(Country)	Day/Month/Year Filed)	Yes	No
No.8-267607	Japan	8/October/1996	☒	☐
(Number)	(Country)	Day/Month/Year Filed)	Yes	No
			☐	☐
(Number)	(Country)	Day/Month/Year Filed)	Yes	No
			☐	☐
(Number)	(Country)	Day/Month/Year Filed)	Yes	No
			☐	☐
(Number)	(Country)	Day/Month/Year Filed)	Yes	No